

TDC Local Command and Global Request Bus V2.1 11/2/00

A local command bus within each TDC input card allows loading new token numbers to each of the input channel INRX FPGA. A global bus extends these commands over all cards, so that the master (output card) can update all the input channels at once. The local command bus is also tied into the VME bus on each card so that diagnostic operation, such as reading or writing memory, reading or writing the token number registers, and clearing or reading the word counters. Both buses are 12 bits with a separate command strobe line and all signals are synchronous to the TDC system clock. Both buses have a multi clock cycle protocol. The local bus uses 3 cycles starting with the command strobe. The input card controller drives the local bus with a command field during the 1st bus cycle and with write data during the 2nd bus cycle. The INRX FPGA drives the bus with read data during the 3rd bus cycle. The global bus uses 6 cycles with a pre-request strobe 2 cycles before the address field. The TDC master controller on the output card drives the global bus during the first 3 bus cycles with Address, Command, and Write Data, and the input card controller on an addressed card drives the global bus during the last 3 cycles with Command, Write Data, and Read Data. The Command and Write Data are copies of the values during the first 3 bus cycles. Addressing schemes allow for individual input channels to be selected, or all channels on one card, or all channels on all cards. In this way the master can update the token numbers of all 36 input channels with one global bus cycle.

GLOBAL BUS CYCLE

Clock Cycle	0	1	2	3	4	5	6	7
CMD STROBE	0	0	0	0	1	0	0	0
LOCAL BUS					Command	Write data	Read data	
Local Bus Source					FPGAPGM CPLD	FPGAPGM CPLD	INRX FPGA	
GPREREQUEST	1	0	0	0	0	0	0	0
GLOBAL BUS			Address	Command	Write data	Command Readback	Write data Readback	Read data
Global Bus Source			SCORE FGPA	SCORE FGPA	SCORE FGPA	FPGAPGM CPLD	FPGAPGM CPLD	FPGAPGM CPLD

LOCAL BUS CYCLE

Clock Cycle	0	1	2
CMD STROBE	1	0	0
LOCAL BUS	Command	Write data	Read data
LOCAL BUS SOURCE	VMEGLP CPLD	VMEGLP CPLD	INRX FPGA

REGISTERS

Register	Register Write Action	Register Read Action
0000	Write NEW TEST token number	Read TEST token number
0001	Write NEW DAQ token number	Read DAQ token number
0010	Write NEW L2 token number	Read L2 token number
0011	Write NEW RXWRITE token number	Read RXWRITE token number
0100	Read RAM @ TEST into TEST buffer	Read TEST word address counter
0101	Read RAM @ DAQ into DAQ HOLD buffer	Read DAQ word address counter
0110	Read RAM @ L2 into L2 HOLD buffer	Read L2 word address counter
0111	Write TEST buffer into RAM @ TEST	Read RXWRITE word address counter
1000	Write TEST buffer	Read TEST buffer
1110	Program FPGA mask register (lower byte)	FPGA status DONE's
1111	Program FPGA data register (lower byte) Set PROGRAM pins high/low (bit 10)	FPGA status INIT's