This homework assignment is essentially a take-home exam, in that it will be weighted like an in-class test. Working in groups is permitted, and all participants will receive full credit for clear, error-free solutions to Parts A and B. However, the penalties for errors will be increased to reflect the number of collaborators. That is, you will benefit from working in groups, but this also raises the performance standard. For both parts of this assignment, the explanation of the work is as important as the solution itself. Evaluating this work is at least as difficult as doing it.

Part A, Due Tuesday November 16

Design and implement the traffic light controller (controller only, do not include the timers) using the simplified FPGA architecture presented in class. Your solution should include:

1. A clear presentation of the design and logic synthesis. A hand-written report is adequate, but the presentation must be easy to understand and read.

2. A layout showing the FPGA implementation, using the FPGA drawing provided. The layout must be clearly labeled for correlation to the design documentation. See the class write-up for an example.

Meet at the regular class time on Tuesday to turn in this work. At that time the solutions will be exchanged.

Part B, Due Tuesday, November 23

Verify the design and implementation of the solution you have been given. Your evaluation should include:

1. A clear description of any errors found in either the design or implementation.
   (a) Design. Is the derivation of implementation logic clearly explained and easy to follow? Was the result correct?
   (b) Implementation. Does the FPGA layout correctly implement the design logic, whether or not that logic was functionally correct?

2. Presentation. Was the documentation adequate to guide the verification task? Was the work made harder by omissions or unclear descriptions of the design process?

Part C (optional), open due date

Create a Foundation library symbol for the FPGA cell in the tutorial write-up, and build an unconnected schematic for the $3 \times 3$ layout used in this assignment.

Build and simulate your solution using these tools. Include a report that explains to others (assume familiarity with the Foundation environment) to use your generic FPGA schematic.