Chapter 5

Interfacing with the Processor
CHAPTER 5. INTERFACING WITH THE PROCESSOR

Figure 5.1: Parallel-to-serial architecture
Figure 5.2: Parallel-to-serial ASM
ARCHITECTURE for UART/S−P

Figure 5.3: Serial-to-parallel architecture
ASM for UART/S−P

Figure 5.4: Serial-to-parallel ASM
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Figure 5.5: Interface signals

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Figure 5.6: Interface ASM
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Carefully analyze all asynchronous control signals for hazards.

General solution, needed if ASM won’t support asynchronous test (e.g. input race).

Figure 5.7: Interface architecture, P→S side.
Carefully analyze all asynchronous control signals for hazards.