MODELLING DIGITAL BUILDING BLOCKS USING THE HENDRIX CONTINUOUS SIMULATION SYSTEM

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OVERVIEW

Almost every event in the world can be viewed as a gradually changing process. Processes are constantly beginning, continuing, or ending, and at any moment one or more processes can be initiated or completed. No process, however, can be completed at the same time it was initiated. Furthermore, the actions of one process can effect the initiation or completion of other processes.

Gary G. Hendrix has developed a system which simulates such "autonomous process dynamics" [2?,160]. This system facilitates modelling events which are independent, but which may effect each other, such as a group of robots moving in a room or an electronic circuit. In this paper, the Hendrix system is used to model the voltage behavior over time of some basic digital hardware building blocks. The material is presented so as to provide insight into the way hardware devices actually work.

The paper begins with a discussion of how signals change from one voltage to another. A simple clock is modelled to illustrate these principles. Next, the other basic unit for understanding digital building blocks, the propagation delay, is explored, and a simple flip-flop is used as an illustration. These basic concepts are then used to implement a model of a mechanical switch, a debouncer for the switch, and a one-shot pulser. The more complicated circuits show the flexibility

of our earlier models. The paper closes with a discussion of how the modelling of hardware building blocks demonstrates the power of the Hendrix system, and a discussion of how this simulation system can be used to explain the operation of digital hardware.

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BACKGROUND

A Brief Description of the Modeling System

The simulation system described by Gary G. Hendrix [3] allows the programmer to model the world as a collection of continuous, ongoing processes. The condition of the world at any time is a list, called the state of the world model (SWM). The SWM is constantly updated with information about the changes occuring within the world itself.

Each process in the Hendrix model is controlled by a scenario. A scenario contains, first, the conditions necessary for the initiation of the process. The initiation conditions, as well as all other conditions in a scenario, are separated into symbolic and numeric conditions. A Symbolic Initiation Condition (ICS) organizes the relationships of the scenario's parameters to the SWM. The Numeric Initiation Conditions (ICN) then restrict the values which may initiate the process. Second, The scenario contains a description of the effects of the process on the SWM, including time dependent equations describing the gradual effects. Ths Symbolic Gradual Effects (EGS) are the symbolic changes in the SWM which take place after the scenario is iniatiated, and which are removed when the scenario terminates. The Numeric Gradual Effects (EGN) contain equations describing the changes in the SWM over time. Hendrix's system views

> time as a continuous phenomenon. Earlier systems contained no parallelism (real or simulated) and omitted the notion of time duration associated with a given process. Continuous time phenomena can be simulated by using mathematical expressions, which are time dependent functions, as parameters. Any reference to such a parameter results in the evaluation of the expression at the given point in model time. [1, p. 1]

The Symbolic Continuation Conditions (CCS) are relations which must exist in the SWM in order for the process to continue. The Numeric Continuation Conditions (CCN) contain equations which evaluate to the time at which the process is to terminate. As long as the CCN or CCS are true, the process continues. When any CCS is removed from the SWM, or the time computed in the CCN is reached, the process will stop.

Each scenario can explicitly alter the SWM through adding and deleting effects. An Initial Adding Effect (EIA) adds relationships to the SWM, while the Initial Deleting Effects (EID) removes relationships from the SWM. This alteration of the world model then may cause other processes to be initiated or terminated. Once a process terminates, the post-deleting effects (EPD) behave like the (EID), removing relationships from the SWM as necessary. Likewise, the post-adding effects (EPA) behave like the EIA, adding relations to the SWM after the termination of the process. Again, these modifications of the SWM may cause other processes to begin or end.

The operations on the SWM caused by the scenarios (adding and deleting effects), the movement of model time, and the actual initiation and termination of processes are all

controlled by a process monitor called the Monitor Executive. This monitor behaves

> as if it were a demon in charge of carrying out all the processes in the modeled world. Given an initial state of the world and a set of process scenarios, the demon determines all processes which would be initiated. For each process to be initiated, the demon selects an imp (a control block) and charges the imp with the realization of the process. As the various imps make changes in the state of the world, the demon watches for new opportunities to start other processes, assigning more imps as needed. When an imp's process is completed or interrupted, the imp notifies the demon who in turn releases the imp from its charge. [3,p.153]

A control block is a particular reference to a scenario, and contains the parameter bindings for that instance of the scenario. Several incarnations of a process can exist simultaneously, and a control block will then be created for each incarnation. The various incarnations can be distinguished by the bindings of the parameters.

Model time, as kept by the process monitor, is not a conventional clock, but rather is a real variable manipulated by the monitor. Each control block has a time at which it will terminate (computed in the CCN). The monitor is constantly scaning the control block list, looking for the control block with the earliest interrupt time (T_i). If no scenario exists with an initiation time less than T_i, time is moved to T_i, and the process is interrupted. Otherwise, any scenario with initiation time less than T_i is begun, with model time moved to the initiation time. [3] For a detailed examination of the program which implements Hendrix's system, see [4].

Basic Concepts

Several steps are necessary when developing a model for use with the Hendrix Simulation System as implemented by Lowrance [4]. In this part of the paper, the rudiments of the modeling system are explored, while giving the reader information about digital circuits and voltage levels. After reading this section, the reader will approach the more complex building blocks with knowledge of voltage levels, signals, propagation delays, and the way these concepts are modeled.

1. The Signal World

The first question to be answered when using the Hendrix System is, "What is the initial state of the world?" When modeling digital hardware, the signal is a crucial element. A signal is an entity which has a voltage level, and which can be an input or an output. Unless it is a constant, a signal can change from a high voltage level to a low voltage level (or vice versa) at a specified rate. These transitions are called edges. Throughout this paper, a high voltage level will be between 2 volts and 5 volts, and a low voltage level will be between 0 volts and 0.8 volts. The SWM for a signal is created by the scenario CREATE-SIGNAL (Figure 1). Any scenario with CREATE in its name is used to create a SWM for the particular entity which is needed. CREATE-SIGNAL

initializes a signal world, and is initiated by adding an ALLOCATE-ACTIVATE CREATE-SIGNAL order to the SWM.(line 1.1.2). The ALLOCATE-ACTIVATE contains the values for the particular signal being created. Line 1.1.4 deletes the ALLOCATE-ACTIVATE

```
.1 (CREATE-SIGNAL(PAR SIG CVOLTS CRATE PT NT PLH PHL)
.2    (ICS(ALLOCATE-ACTIVATE CREATE-SIGNAL SIG CVOLTS CRATE PT NT
.3           PLH PHL))
.4    (EID(ALLOCATE-ACTIVATE CREATE-SIGNAL SIG CVOLTS CRATE PT NT
.5           PLH PHL))
.6    (EIA(TYPE SIG SIGNAL)(VOLTS SIG CVOLTS)(RORIN SIG CRATE)
.7        (PTHRESH SIG PT)(NTHRESH SIG NT)
.8        (PULSEUP SIG OFF)(PULSEDN SIG OFF)
.9        (PLHIN SIG PLH)(PHLIN SIG PHL)))
```

Figure 1.1

order, so that only one signal is created. Lines 1.1.6 through 1.1.9 create a SWM where SIG is a signal, SIG has a voltage level of CVOLTS, and a rate of voltage transition CRATE (where the voltage transition rate is CRATE volts per nanosecond). Since many digital devices are triggered or started by the transitions or edges of signals, the relations on line 1.1.7 are added to the SWM. (PTHRESH SIG PT) means that when the voltage of the signal SIG rises to PT volts (the positive threshold), a message (PULSEUP SIG ON) is inserted in the SWM. This enables the modeller to use upward transitions of the signal SIG in the model. The relation (NTHRESH SIG NT) causes a (PULSEDN SIG ON) to be added to the SWM when SIG falls to NT (the negative threshold). When SIG is created, it is neither rising or falling (line1.1.8), it has a low to high propagation delay PLH (line1.1.9), and it has a high to low propagation delay PHL. The concept of

propagation delay will be explored in section three, the Propagation Delay World.

Now, the scenarios which will perform the transitions between high and low voltage levels are written. The scenerios STARTUP and FINISHUP (Figure 1.2) are written. The scenerio STARTUP will be used as an example, since design of the other scenarios is similar.

```
.1  (STARTUP(PAR S CVOLTS : CRORIN CPTHRESH)
.2     (ICS(TYPE S SIGNAL)(VOLTS S CVOLTS)(RORIN S CRORIN)
.3        (PTHRESH S CPTHRESH)(PULSEUP S OFF)(EDGE S UP))
.4     (ICN(LT CVOLTS CPTHRESH)(GE CVOLTS 0)(GE CRORIN 0.000001))
.5     (EID(VOLTS S *)(EDGE S UP))
.6     (EGS(VOLTS S YVOLTS))
.7     (EGN((:= YVOLTS(*PLUS CVOLTS(*TIMES CRORIN $)))
.8          (:= $ (QUO(*DIF YVOLTS CVOLTS)CRORIN))))
.9     (CCN FUNC (*PLUS %(QUO(*DIF CPTHRESH CVOLTS)CRORIN)))
.10    (EPD(PULSEUP S OFF)(VOLTS S *))
.11    (EPA(PULSEUP S ON)(VOLTS S CPTHRESH)))

.12 (FINISHUP(PAR S CVOLTS : CRORIN CPTHRESH)
.13    (ICS(TYPE S SIGNAL)(VOLTS S CVOLTS)(RORIN S CRORIN)
.14       (PTHRESH S CPTHRESH)(PULSEUP S ON))
.15    (ICN(EQUAL CVOLTS CPTHRESH)(GE CRORIN 0.000001))
.16    (EID(VOLTS S *))
.17    (EGS(VOLTS S YVOLTS))
.18    (EGN((:= YVOLTS (*PLUS CVOLTS (*TIMES CRORIN $)))
.19         (:= $ (QUO(*DIF YVOLTS CVOLTS) CRORIN))))
.20    (CCN FUNC (*PLUS %(QUO(*DIF 3.4 CVOLTS) CRORIN)))
.21    (EPD(PULSEUP S ON))
.22    (EPA(PULSEUP S OFF)))
```

Figure 1.2

The scenario performs a gradual task of raising the voltage level of the signal. This rising voltage is produced by the following equation:

$$YVOLTS = CVOLTS + (CRORIN * \$)$$

where YVOLTS is the gradually increasing voltage level, CVOLTS is the initial voltage level when the scenario is entered,

CRORIN is the rate of voltage rise, and $ is the model time elapsed since the scenario began. All of this in incorporated into the gradual conditions of the scenario (lines 1.2.6-1.2.8).

The next step is to find a formula for determining the proper time to interrupt or stop the scenario. The equation is:

INTERRUPT TIME = % + (CPTHRESH-CVOLTS)/CRORIN,

where % is the process initiation time, and CPTHRESH is the positive threshold of the signal. Since it is at this time that the voltage has reached thethreshold level, the signal (PULSEUP S ON) is added to the SWM (lines 1.2.9-1.2.11).

The third step in the formation of the secnario STARTUP is to create the initial conditions of the scenario. (lines 1.2.2-1.2.4). The first five conditions are part of the initial SWM, and can be true for all signals in the world being modelled. However, it is the last condition that has to be true before the scenario is initiated for the signal S. This condition, (EDGE S UP), makes the initiation of the scenario unique, and allows other scenarios to trigger signals.

Finally, pre- and post-effects are added to the scenario. (lines 1.2.5, and 1.2.10-11). The EID removes the current voltage of the signal S, and the condition that S is rising. Once the time computed on line 1.2.9 is reached, the EPD removes the condition (PULSEUP S OFF) and the voltage level of S. The condition (PULSEUP S ON), as well as the condition that S has reached the threshold voltage level, is added to the SWM in line 1.2.11 of the scenario.

The scenario FINISHUP uses the relations (PULSEUP S ON) and (VOLTS S CPTHRESH), line 1.2.14, as its unique initiation conditions. It then raises the voltage of the signal S to the proper high level of 3.4 volts, deleting the (PULSEUP S ON) when this level is reached. The opposite pair of scenarios, STARTDN and FINISHDN (Figure 1.3), use analogous methods to gradually bring the voltage level to a low state.

```
(STARTDN(PAR S CVOLTS : CRORIN CNTHRESH)
   (ICS(TYPE S SIGNAL)(VOLTS S CVOLTS)(RORIN S CRORIN)
       (NTHRESH S CNTHRESH)(PULSEDN S OFF)(EDGE S DN))
   (ICN(GT CVOLTS CNTHRESH)(LT CVOLTS 5)(GE CRORIN 0.000001))
   (EID(VOLTS S *)(EDGE S DN))
   (EGS(VOLTS S YVOLTS))
   (EGN((:= YVOLTS(*DIF CVOLTS(*TIMES CRORIN $)))
        (:= $ (QUO(*DIF CVOLTS YVOLTS)CRORIN))))
   (CCN FUNC (*PLUS %(QUO(*DIF CVOLTS CNTHRESH)CRORIN)))
   (EPD(PULSEDN S OFF)(VOLTS S *))
   (EPA(PULSEDN S ON)(VOLTS S CNTHRESH)))

(FINISHDN(PAR S CVOLTS : CRORIN CNTHRESH)
   (ICS(TYPE S SIGNAL)(VOLTS S CVOLTS)(RORIN S CRORIN)
       (NTHRESH S CNTHRESH)(PULSEDN S ON))
   (ICN(EQUAL CVOLTS CNTHRESH)(GE CRORIN 0.000001))
   (EID(VOLTS S *))
   (EGS(VOLTS S YVOLTS))
   (EGN((:= YVOLTS(*DIF CVOLTS(*TIMES CRORIN $)))
        (:= $(QUO(*DIF CVOLTS YVOLTS)CRORIN))))
   (CCN FUNC (*PLUS % (QUO(*DIF CVOLTS 0.2)CRORIN)))
   (EPD(PULSEDN S ON))
   (EPA(PULSEDN S OFF)))
```

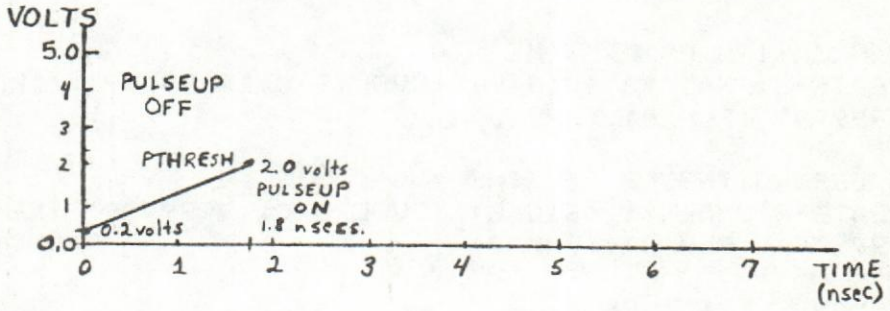
Figure 1.3

Example 1 illustrates thechanges in the SWM caused by adding a rising edge to thesignal world. The control block trace shows the creation and destruction of the STARTUP and FINISHUP scenarios, the parameter bindings, and the model time at initiation or interuption. The changing voltage of the signal S is found under the ****SKLRS**** section, while the pulse is rising, but the final value is returned to the ****EXPRS**** part of the SWM.

Example one -- The Signal World

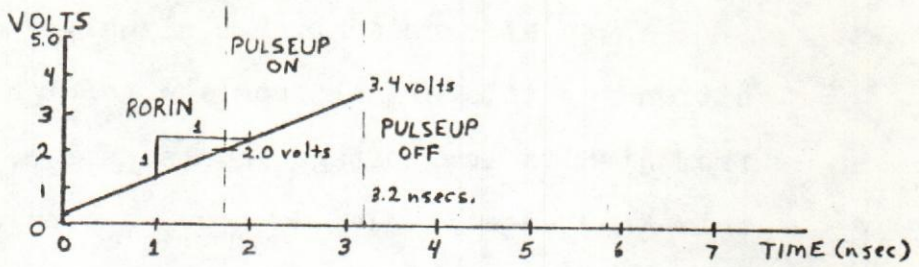
```
*(HSIM)

============================
HENDRIX SIMULATION SYSTEM
============================

INPUT SCENARIO LIST: *(EVAL SLIST)

STARTUP FINISHUP STARTDN FINISHDN CREATE-SIGNAL

INPUT SWM RELATION LIST: *(EVAL SWM)


COMMAND: *(TRACE *)


COMMAND: *AUTOSNAP


COMMAND: *(ADD(ALLOCATE-ACTIVATE CREATE-SIGNAL S 0.2 1 2 0.8 0 0))


COMMAND: *GO


<<<CREATING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG S) (CVOLTS 0.19999999) (CRATE 1) (PT 2) (NT 0.7
9999999) (PLH 0) (PHL 0)

<<<DESTROYING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG S) (CVOLTS 0.19999999) (CRATE 1) (PT 2) (NT 0.7
9999999) (PLH 0) (PHL 0)

COMMAND: *PICTURE


****TIME****
0
****EXPRS****
(PHLIN S 0)
(PLHIN S 0)
(PULSEDN S OFF)
(PULSEUP S OFF)
(NTHRESH S 0.79999999)
(PTHRESH S 2)
(RORIN S 1)
(VOLTS S 0.19999999)
(TYPE S SIGNAL)
****SKLRS****
**********

COMMAND: *(ADD(EDGE S UP))
```

```
COMMAND: *GO

<<<CREATING CB>>> TIME = 0
STARTUP ** (S S) (CVOLTS 0.19999999) (CRORIN 1) (CPTHRESH 2)

****TIME****
0
****EXPRS****
(PHLIN S 0)
(PLHIN S 0)
(PULSEDN S OFF)
(PULSEUP S OFF)
(NTHRESH S 0.79999999)
(PTHRESH S 2)
(RORIN S 1)
(TYPE S SIGNAL)
****SKLRS****
(VOLTS S 0.19999999)
**********

<<<DESTROYING CB>>> TIME = 1.7999999
STARTUP ** (S S) (CVOLTS 0.19999999) (CRORIN 1) (CPTHRESH 2)

<<<CREATING CB>>> TIME = 1.7999999
FINISHUP ** (S S) (CVOLTS 2) (CRORIN 1) (CPTHRESH 2)

****TIME****
1.7999999
****EXPRS****
(PHLIN S 0)
(PLHIN S 0)
(PULSEDN S OFF)
(PULSEUP S ON)
(NTHRESH S 0.79999999)
(PTHRESH S 2)
(RORIN S 1)
(TYPE S SIGNAL)
****SKLRS****
(VOLTS S 2.0)
**********
```

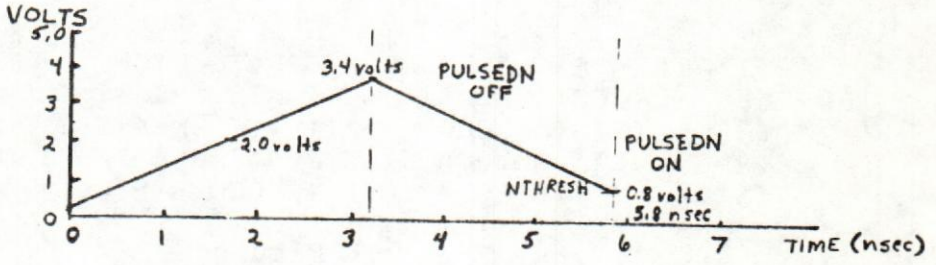



```
<<<DESTROYING CB>>> TIME = 3.2000000
FINISHUP ** (S S) (CVOLTS 2) (CRORIN 1) (CPTHRESH 2)

COMMAND: *(ADD(EDGE S DN))

COMMAND: *GO

<<<CREATING CB>>> TIME = 3.2000000
STARTDN ** (S S) (CVOLTS 3.4000000) (CRORIN 1) (CNTHRESH 0.79999999)
```

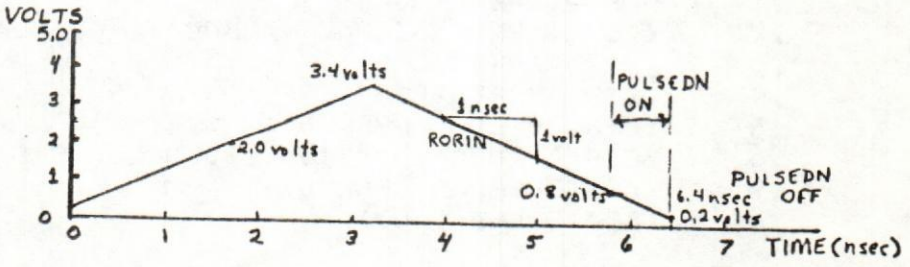
```
****TIME****
3.2000000
****EXPRS****
(PHLIN S 0)
(PLHIN S 0)
(PULSEDN S OFF)
(PULSEUP S OFF)
(NTHRESH S 0.79999999)
(PTHRESH S 2)
(RORIN S 1)
(TYPE S SIGNAL)
****SKLRS****
(VOLTS S 3.4000000)
******************
```




```
<<<DESTROYING CB>>> TIME = 5.8000000
STARTDN ** (S S) (CVOLTS 3.4000000) (CRORIN 1) (CNTHRESH 0.79999999)

<<<CREATING CB>>> TIME = 5.8000000
FINISHDN ** (S S) (CVOLTS 0.79999999) (CRORIN 1) (CNTHRESH 0.79999999
)

****TIME****
5.8000000
****EXPRS****
(PHLIN S 0)
(PLHIN S 0)
(PULSEDN S ON)
(PULSEUP S OFF)
(NTHRESH S 0.79999999)
(PTHRESH S 2)
(RORIN S 1)
(TYPE S SIGNAL)
****SKLRS****
(VOLTS S 0.79999999)
******************
```




```
<<<DESTROYING CB>>> TIME = 6.4000000
FINISHDN ** (S S) (CVOLTS 0.79999999) (CRORIN 1) (CNTHRESH 0.79999999
)

COMMAND: *PICTURE


****TIME****
6.4000000
****EXPRS****
(PHLIN S 0)
(PLHIN S 0)
(PULSEDN S OFF)
(PULSEUP S OFF)
(NTHRESH S 0.79999999)
(PTHRESH S 2)
(RORIN S 1)
(VOLTS S 0.19999997)
(TYPE S SIGNAL)
****SKLRS****
******************

COMMAND: *STOP

(****TERMINATED-AT-TIME**** 6.4000000)
```



2. The Clock World

A way of representing a signal, and the means of transition for this signal from low to high voltage levels, and from high to low voltage levels have now been established. This knowledge is used to model a specialized signal -- the clock. A clock signal is a signal that, once it is turned on, oscillates between high and low voltage at a given rate of speed. To model this, a timing mechanism to switch the signal back and forth has been provided.

The first part of the Clock World is a CREATE scenario for the clock, which can be found in Figure 2.1. An

```
.1 (CREATE-CLOCK(PAR SIG RATE PT NT)
.2    (ICS(ALLOCATE-ACTIVATE CREATE-CLOCK SIG RATE PT NT))
.3    (EID(ALLOCATE-ACTIVATE CREATE-CLOCK SIG RATE PT NT))
.4    (EIA(ALLOCATE-ACTIVATE CREATE-SIGNAL SIG 0.2 RATE PT NT 0 0)
.5       (SPEED SIG 0)(CLOCK SIG LOW)))
```

Figure 2.1

ALLOCATE-ACTIVATE order is necessary to initiate the clock (line 2.1.2). This order says the clock world contains a signal SIG, with voltage transition rate RATE, a positive threshold PT, and a negative threshold NT. CREATE-CLOCK removes the ALLOCATE-ACTIVATE order, as in the signal world, and then creates a signal (line2.1.4). The conditions on line 2.1.5 are the initiation condition for CLOCKON.

```
.1 (CLOCKON(PAR C CSPEED)
.2    (ICS(TYPE C SIGNAL)(ALLOCATE-ACTIVATE CLOCKON C CSPEED)
.3         (SPEED C 0))
.4    (EID (SPEED C 0))
.5    (EIA(SPEED C CSPEED))
.6    (CCS(ALLOCATE-ACTIVATE CLOCKON C CSPEED))
.7    (EPD(SPEED C CSPEED))
.8    (EPA(SPEED C 0)))
```

Figure 2.2

The scenario CLOCKON (Figure 2.2) turns the clock on or off. An ALLOCATE-ACTIVATE order (line 2.1.2) includes the desired clock speed, initiates CLOCKON. As long as the ALLOCATE-ACTIVATE order remains in the SWM, the clock will continue to oscillate at a rate CSPEED. When the ALLOCATE-ACTIVATE order is deleted, the clock turns off, and the clock speed is reset to zero. Throughout the remainder of this paper, a clock speed of one MHz (one million cycles per second) will be assumed. The scenario HIGHCLOCK (Figure 2.3) will keep

```
.1  (HIGHCLOCK(PAR C : CSPEED CVOLTS)
.2     (ICS(CLOCK C HIGH)(TYPE C SIGNAL)(VOLTS C CVOLTS)(SPEED C CSPEED)
.3     (ICN(GE CVOLTS 3.4)(LE CVOLTS 5.0)(GE CSPEED 0.001)
.4        (LE CSPEED 10))
.5     (CCN FUNC (*PLUS % (QUO 500 CSPEED)))
.6     (EPD(CLOCK C HIGH))
.7     (EPA(EDGE C DN)(CLOCK C LOW)))
```

Figure 2.3

the signal high for one-half the clock's cycle time in nanoseconds. Once this scenario is entered, the clock signal will remain high until a time 500 / CSPEED has passed (line 2.3.5). This formula is derived as follows. CSPEED is in units of MHz, which equals one cycle in 1000 nanoseconds. Thus, 1/2 cycle would be 500 nanoseconds. Five hundred divided by the CSPEED will equal how many nanoseconds the clock should remain in its current state.

```
.1  (LOWCLOCK(PAR C : CSPEED CVOLTS)
.2     (ICS(CLOCK C LOW)(TYPE C SIGNAL)(VOLTS C CVOLTS)(SPEED C CSPEED))
.3     (ICN(GE CVOLTS 0)(LE CVOLTS 0.8)(GE CSPEED 0.001)
.4        (LE CSPEED 10))
.5     (CCN FUNC (*PLUS % (QUO 500 CSPEED)))
.6     (EPD(CLOCK C LOW))
.7     (EPA(EDGE C UP)(CLOCK C HIGH)))
```

Figure 2.4

When this time has passed, the relation (EDGE CLK DN) is added to the SWM to start the transition to the low level. The scenario LOWCLOCK (Figure 2.4) behaves in a similar manner.

The operation of the clock is demonstrated in example 2. The (ALLOCATE-ACTIVATE CLOCKON CLK 1) order starts the clock. The trace then shows the initiation and destruction of the STARTUP and FINISHUP scenarios. The listing of the SWM shows that now the clock CLK is high. The trace continues to show the oscillation of the clock signal until the ALLOCATE-ACTIVATE order is deleted.

Example two -- The Clock World

```
*(HSIM)

==========================
HENDRIX SIMULATION SYSTEM
==========================

INPUT SCENARIO LIST: *(EVAL SLIST)

HIGHCLOCK LOWCLOCK CLOCKON STARTUP FINISHUP STARTDN FINISHDN
CREATE-SIGNAL CREATE-CLOCK

INPUT SWM RELATION LIST: *(EVAL SWM)


COMMAND: *(TRACE *)


COMMAND: *(SNAPSHOT 50)


COMMAND: *(SNAPSHOT 502)


COMMAND: *(SNAPSHOT 550)


COMMAND: *(SNAPSHOT 1006)


COMMAND: *(SNAPSHOT 1010)


COMMAND: *(ADD(ALLOCATE-ACTIVATE CREATE-CLOCK CLK 1 1.4 1.4))


COMMAND: *GO


<<<CREATING CB>>> TIME = 0
CREATE-CLOCK ** (SIG CLK) (RATE 1) (PT 1.4000000) (NT 1.4000000)

<<<DESTROYING CB>>> TIME = 0
CREATE-CLOCK ** (SIG CLK) (RATE 1) (PT 1.4000000) (NT 1.4000000)

<<<CREATING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG CLK) (CVOLTS 0.19999999) (CRATE 1) (PT 1.400000
0) (NT 1.4000000) (PLH 0) (PHL 0)

<<<DESTROYING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG CLK) (CVOLTS 0.19999999) (CRATE 1) (PT 1.400000
0) (NT 1.4000000) (PLH 0) (PHL 0)

COMMAND: *(BREAK 1700)


COMMAND: *(ADD(ALLOCATE-ACTIVATE CLOCKON CLK 1))


COMMAND: *GO
```

```
<<<CREATING CB>>> TIME = 0
CLOCKON ** (C CLK) (CSPEED 1)

<<<CREATING CB>>> TIME = 0
LOWCLOCK ** (C CLK) (CSPEED 1) (CVOLTS 0.19999999)

****TIME****
50
****EXPRS****
(PHLIN CLK 0)
(PLHIN CLK 0)
(PULSEDN CLK OFF)
(PULSEUP CLK OFF)
(NTHRESH CLK 1.4000000)
(PTHRESH CLK 1.4000000)
(RORIN CLK 1)
(VOLTS CLK 0.19999999)
(TYPE CLK SIGNAL)
(CLOCK CLK LOW)
(SPEED CLK 1)
(ALLOCATE-ACTIVATE CLOCKON CLK 1)
****SKLRS****
**********

<<<DESTROYING CB>>> TIME = 500.0
LOWCLOCK ** (C CLK) (CSPEED 1) (CVOLTS 0.19999999)

<<<CREATING CB>>> TIME = 500.0
STARTUP ** (S CLK) (CVOLTS 0.19999999) (CRORIN 1) (CPTHRESH 1.4000000
)

<<<DESTROYING CB>>> TIME = 501.20000
STARTUP ** (S CLK) (CVOLTS 0.19999999) (CRORIN 1) (CPTHRESH 1.4000000
)

<<<CREATING CB>>> TIME = 501.20000
FINISHUP ** (S CLK) (CVOLTS 1.4000000) (CRORIN 1) (CPTHRESH 1.4000000
)

****TIME****
502.0000
****EXPRS****
(PHLIN CLK 0)
(PLHIN CLK 0)
(PULSEDN CLK OFF)
(PULSEUP CLK ON)
(NTHRESH CLK 1.4000000)
(PTHRESH CLK 1.4000000)
(RORIN CLK 1)
(TYPE CLK SIGNAL)
(CLOCK CLK HIGH)
(SPEED CLK 1)
(ALLOCATE-ACTIVATE CLOCKON CLK 1)
****SKLRS****
(VOLTS CLK 1.4000000)
**********

<<<DESTROYING CB>>> TIME = 503.20000
FINISHUP ** (S CLK) (CVOLTS 1.4000000) (CRORIN 1) (CPTHRESH 1.4000000
)
```

```
<<<CREATING CB>>> TIME = 503.20000
HIGHCLOCK ** (C CLK) (CSPEED 1) (CVOLTS 3.4000000)

****TIME****
550.00000
****EXPRS****
(PHLIN CLK 0)
(PLHIN CLK 0)
(PULSEDN CLK OFF)
(PULSEUP CLK OFF)
(NTHRESH CLK 1.4000000)
(PTHRESH CLK 1.4000000)
(RORIN CLK 1)
(VOLTS CLK 3.4000000)
(TYPE CLK SIGNAL)
(CLOCK CLK HIGH)
(SPEED CLK 1)
(ALLOCATE-ACTIVATE CLOCKON CLK 1)
****SKLRS****
**********

<<<DESTROYING CB>>> TIME = 1003.2000
HIGHCLOCK ** (C CLK) (CSPEED 1) (CVOLTS 3.4000000)

<<<CREATING CB>>> TIME = 1003.2000
STARTDN ** (S CLK) (CVOLTS 3.4000000) (CRORIN 1) (CNTHRESH 1.4000000)


<<<DESTROYING CB>>> TIME = 1005.2000
STARTDN ** (S CLK) (CVOLTS 3.4000000) (CRORIN 1) (CNTHRESH 1.4000000)


<<<CREATING CB>>> TIME = 1005.2000
FINISHDN ** (S CLK) (CVOLTS 1.4000000) (CRORIN 1) (CNTHRESH 1.4000000
)

****TIME****
1006.0000
****EXPRS****
(PHLIN CLK 0)
(PLHIN CLK 0)
(PULSEDN CLK ON)
(PULSEUP CLK OFF)
(NTHRESH CLK 1.4000000)
(PTHRESH CLK 1.4000000)
(RORIN CLK 1)
(TYPE CLK SIGNAL)
(CLOCK CLK LOW)
(SPEED CLK 1)
(ALLOCATE-ACTIVATE CLOCKON CLK 1)
****SKLRS****
(VOLTS CLK 1.4000000)
**********

<<<DESTROYING CB>>> TIME = 1006.4000
FINISHDN ** (S CLK) (CVOLTS 1.4000000) (CRORIN 1) (CNTHRESH 1.4000000
)
```

```
<<<CREATING CB>>> TIME = 1006.4000
LOWCLOCK ** (C CLK) (CSPEED 1) (CVOLTS 0.20000305)

****TIME****
1010.0000
****EXPRS****
(PHLIN CLK 0)
(PLHIN CLK 0)
(PULSEDN CLK OFF)
(PULSEUP CLK OFF)
(NTHRESH CLK 1.4000000)
(PTHRESH CLK 1.4000000)
(RORIN CLK 1)
(VOLTS CLK 0.20000305)
(TYPE CLK SIGNAL)
(CLOCK CLK LOW)
(SPEED CLK 1)
(ALLOCATE-ACTIVATE CLOCKON CLK 1)
****SKLRS****
****************


<<<DESTROYING CB>>> TIME = 1506.4000
LOWCLOCK ** (C CLK) (CSPEED 1) (CVOLTS 0.20000305)

<<<CREATING CB>>> TIME = 1506.4000
STARTUP ** (S CLK) (CVOLTS 0.20000305) (CRORIN 1) (CPTHRESH 1.4000000
)

<<<DESTROYING CB>>> TIME = 1507.6000
STARTUP ** (S CLK) (CVOLTS 0.20000305) (CRORIN 1) (CPTHRESH 1.4000000
)

<<<CREATING CB>>> TIME = 1507.6000
FINISHUP ** (S CLK) (CVOLTS 1.4000000) (CRORIN 1) (CPTHRESH 1.4000000
)

<<<DESTROYING CB>>> TIME = 1509.6000
FINISHUP ** (S CLK) (CVOLTS 1.4000000) (CRORIN 1) (CPTHRESH 1.4000000
)

==============================
>>>BREAK AT 1700
==============================

COMMAND: *(DEL(ALLOCATE-ACTIVATE * * *))


<<<DESTROYING CB>>> TIME = 1700
CLOCKON ** (C CLK) (CSPEED 1)

COMMAND: *GO

==============================

<<<DESTROYING CB>>> TIME = 2009.6000
HIGHCLOCK ** (C CLK) (CSPEED 1) (CVOLTS 3.4000000)

<<<CREATING CB>>> TIME = 2009.6000
STARTDN ** (S CLK) (CVOLTS 3.4000000) (CRORIN 1) (CNTHRESH 1.4000000)
```

```
<<<DESTROYING CB>>> TIME = 2011.6000
STARTDN ** (S CLK) (CVOLTS 3.4000000) (CRORIN 1) (CNTHRESH 1.4000000)

<<<CREATING CB>>> TIME = 2011.6000
FINISHDN ** (S CLK) (CVOLTS 1.4000000) (CRORIN 1) (CNTHRESH 1.4000000
)

<<<DESTROYING CB>>> TIME = 2012.8000
FINISHDN ** (S CLK) (CVOLTS 1.4000000) (CRORIN 1) (CNTHRESH 1.4000000
)

COMMAND: *STOP

(****TERMINATED-AT-TIME**** 2012.8000)
```

3. The Propagation Delay World

Many of the concepts necessary for modelling a signal can be applied when modelling hardware gates and storage elements. The first process to be simulated is the propagation delay through a gate. Propagation delay is the very short period of time between when the inputs to a circuit change, and when the output recognizes this change. To a person using an integrated circuit, this presents little or no problem because the delay is usually less than 100 nanoseconds. When modelling on the nanosecond level, however, this propagation delay becomes very important, especially since the delay is usually different for the low to high transition and for the high to low transition of the output.

The scenarios PROPDELAYLH and PROPDELAYHL (Figure 3.1) accomplish this task for low to high transitions and for high to low transitions of the output, respectively.

```
.1  (PROPDELAYLH(PAR Q L : CPLHIN CRORIN CVOLTS CPTHRESH)
.2     (ICS(PLHIN Q CPLHIN)(TRIGLH Q L)(RORIN L CRORIN)
.3        (VOLTS L CVOLTS)(PTHRESH L CPTHRESH))
.4     (EID(TRIGLH Q L))
.5     (CCN FUNC (*PLUS % (*DIF CPLHIN(QUO (*DIF CPTHRESH CVOLTS)
.6                                  CRORIN))))
.7     (EPA(EDGE L UP)))

.8  (PROPDELAYHL(PAR Q Z : CPHLIN CRORIN CVOLTS CNTHRESH)
.9     (ICS(PHLIN Q CPHLIN)(TRIGHL Q Z)(RORIN Z CRORIN)
.10       (VOLTS Z CVOLTS)(NTHRESH Z CNTHRESH))
.11    (EID(TRIGHL Q Z))
.12    (CCN FUNC (*PLUS %(*DIF CPHLIN (QUO (*DIF CVOLTS CNTHRESH)
.13                                  CRORIN))))
.14    (EPA(EDGE Z DN)))
```

Figure 3.1

When the pseudo-relation (TRIGLH Q L), line3.1.2, is found in the SWM, the scenario PROPDELAYLH waits for the propagation

delay time (PLHIN), and then uses the pseudo-relation (EDGE L UP), line 3.1.7, to cause the signal to rise. (A pseudo-relation is a relation which is used only to initiate desired scenarios. A pseudo-relation will never be found in the SWM when a PICTURE is taken.) In the CCN, the time (CPTHRESH-CVOLTS)/CRORIN is subtracted from the given propagation delay time. This is necessary because of the effect shown in Figure 3.2. The total propagation delay time lasts until the output signal has reached the threshold level. By subtracting the time it would take the signal to reach the threshold level, we get an accurate time to delay before starting the signal upward.

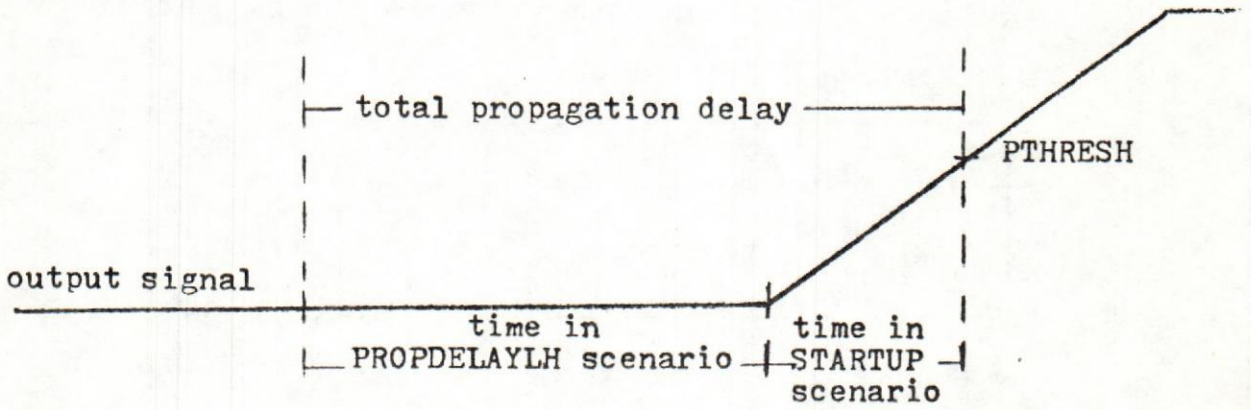


Figure 3.2

4. The Flip-Flop World

The type D flip-flop is a hardware device which has the characteristic of memory. When a type D flip-flop senses a rising clock edge, the voltage on its input is duplicated on its Q output, and the inverse voltage is placed on its Q' output. The rising clock edge is a product of the scenario STARTUP (Figure 1.2), and the event associated with this occurence is called triggering the flip-flop. Between clock pulses, the outputs Q and Q' remain stable, even when the value at D fluctuates. A type D flip-flop, then delays a signal for one clock period. D flip-flops are commonly used for data storage, and also for data synchronization. [7] Figure 4.1 is the truth table and the functional diagram for a type D flip-flop. [6, p.5-22]

FUNCTION TABLE			
D	CLK	Q	Q
L	↑	L	H
H	↑	H	L
X	L	Q	Q
X	H	Q	Q

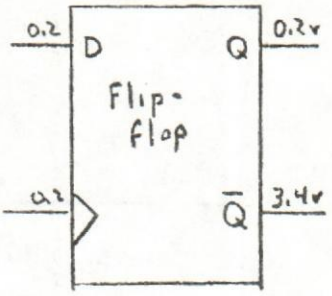


Figure 4.1

When modelling the behavior of this flip-flop, only the two cases where the clock trigger occurs when the input D is the inverse of the output Q must be considered, since if the new input is the same as the output, no propagation delay will result. One scenario (FFOUTLOW, Figure 4.2) then models the flip-flop output's transition from high to low, and one scenario (FFOUTHIGH, Figure 4.3) models the change from low to high. The ICS for each scenario (lines 4.2.2, 4.3.2)

contain the voltage levels necessary to initate a change in the D input, the voltage levels necessary to initiate a change in the Q output, and the condition that the clock is producing a rising edge. The ICN (lines 4.2.4,4.3.4) ~~the~~ list the voltage levels required to initiate the scenario. Each scenario then deletes the current output, (lines 4.2.7,4.3.7) and initiates the proper propagation delay scenaric.(lines 4.2.8, 4.3.8).

```
.1 (FFOUTLOW(PAR CLK1 DIN Q QNOT : CDIN CQ CQNOT)
.2    (ICS(TUPLE CLK1 DIN Q QNOT)(PULSEUP CLK1 ON)(STATE Q HIGH)
.3        (VOLTS DIN CDIN)(VOLTS Q CQ)(VOLTS QNOT CQNOT))
.4    (ICN(GE CDIN 0.2)(LE CDIN 0.8)
.5        (GE CQ 2)(LE CQ 5)
.6        (GE CQNOT 0.2)(LE CQNOT 0.8))
.7    (EID(STATE Q HIGH))
.8    (EIA(STATE Q LOW)(TRIGLH DIN QNOT)(TRIGHL DIN Q)))
```

Figure 4.2

```
.1 (FFOUTHIGH(PAR CLK1 DIN Q QNOT : CDIN CQ CQNOT)
.2    (ICS(TUPLE CLK1 DIN Q QNOT)(PULSEUP CLK1 ON)(STATE Q LOW)
.3        (VOLTS DIN CDIN)(VOLTS Q CQ)(VOLTS QNOT CQNOT))
.4    (ICN(GE CDIN 2.0)(LE CDIN 5.0)
.5        (GE CQ 0)(LE CQ 0.8)
.6        (GE CQNOT 2.0)(LE CQNOT 5.0))
.7    (EID(STATE Q LOW))
.8    (EIA(STATE Q HIGH)(TRIGLH DIN Q)(TRIGHL DIN QNOT)))
```

Figure 4.3

The SWM for the flip-flop is created by the scenario, CREATE-FLIP-FLOP (Figure 4.4). It uses the CREATE-SIGNAL scenario to create the input signal and the output signals (lines 4.4.4-6). It also creates a clock input to the flip-flop by initializing CREATE-CLOCK. The relation (TUPLE K I O1 O2) (line 4.4.8) is then added to the SWM to link the four signals together into one circuit. This allows for more than one flip-flop to be modeled at the same time. The final relation

added to the SWM is the state of the output which is used in the FFOUTHIGH and FFOUTLOW scenarios to prevent them from being reinitialized while the propagation delays occur.

```
.1 (CREATE-FLIP-FLOP (PAR K I O1 O2 VI VO1 VO2 STO1)
.2    (ICS(ALLOCATE-ACTIVATE CREATE-FLIP-FLOP K I O1 O2 VI VO1 VO2
              STO1))
.3    (EID(ALLOCATE-ACTIVATE CREATE-FLIP-FLOP K I O1 O2 VI VO1 VO2
              STO1))
.4    (EIA(ALLOCATE-ACTIVATE CREATE-SIGNAL I VI 1 2.0 0.8 14 20)
.5        (ALLOCATE-ACTIVATE CREATE-SIGNAL O1 VO1 1 2.0 0.8 0 0)
.6        (ALLOCATE-ACTIVATE CREATE-SIGNAL O2 VO2 1 2.0 0.8 0 0)
.7        (ALLOCATE-ACTIVATE CREATE-CLOCK K 1 2.0 0.8)
.8        (TUPLE K I O1 O2)
.9        (STATE O1 STO1)))
```

Figure 4.4

Example 3 is a sample output which shows the behavior of the flip-flop scenarios. When the SWM is first created, the voltage levels of the input IN1 and the output OUT1 are both low. Then the voltage level of IN1 is changed to a high state and the clock, CLK, is turned on. When the upward clock edge occurs (TIME = 501.7999), the scenario FFOUTHIGH is initiated, causing the propagation delays to begin and changing the state of OUT1 to a HIGH level. After the propagation delays, the flip-flop is stabilized with the input, IN1, and the output, OUT1, again at the same voltage level. OUT1 will remain stable until at least the next clock pulse and it will only change then if the level of IN1 is a low voltage.

Example three -- the Flip-flop World

```
*(HSIM)

==========================
HENDRIX SIMULATION SYSTEM
==========================

INPUT SCENARIO LIST: *(EVAL SLIST)

HIGHCLOCK LOWCLOCK CLOCKON STARTUP FINISHUP STARTDN FINISHDN FFOUTHIGH
FFOUTLOW PROPDELAYLH PROPDELAYHL
CREATE-SIGNAL CREATE-CLOCK CREATE-FLIP-FLOP

INPUT SWM RELATION LIST: *(EVAL SWM)


COMMAND: *(TRACE *)


COMMAND: *(SNAPSHOTS 50 502 510 550)



COMMAND: *(BREAK 800)


COMMAND: *(ADD(ALLOCATE-ACTIVATE CREATE-FLIP-FLOP CLK IN1 OUT1 OUT2 0.2
 0.2 3.4 LOW))


COMMAND: *GO


<<<CREATING CB>>> TIME = 0
CREATE-FLIP-FLOP ** (K CLK) (I IN1) (O1 OUT1) (O2 OUT2) (VI 0.1999999
9) (VO1 0.19999999) (VO2 3.4000000) (STO1 LOW)

<<<DESTROYING CB>>> TIME = 0
CREATE-FLIP-FLOP ** (K CLK) (I IN1) (O1 OUT1) (O2 OUT2) (VI 0.1999999
9) (VO1 0.19999999) (VO2 3.4000000) (STO1 LOW)

<<<CREATING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG OUT2) (CVOLTS 3.4000000) (CRATE 1) (PT 2.0) (NT
 0.79999999) (PLH 0) (PHL 0)

<<<DESTROYING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG OUT2) (CVOLTS 3.4000000) (CRATE 1) (PT 2.0) (NT
 0.79999999) (PLH 0) (PHL 0)

<<<CREATING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG OUT1) (CVOLTS 0.19999999) (CRATE 1) (PT 2.0) (N
T 0.79999999) (PLH 0) (PHL 0)
```

```
<<<DESTROYING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG OUT1) (CVOLTS 0.19999999) (CRATE 1) (PT 2.0) (N
T 0.79999999) (PLH 0) (PHL 0)

<<<CREATING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG IN1) (CVOLTS 0.19999999) (CRATE 1) (PT 2.0) (NT
 0.79999999) (PLH 14) (PHL 20)

<<<DESTROYING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG IN1) (CVOLTS 0.19999999) (CRATE 1) (PT 2.0) (NT
 0.79999999) (PLH 14) (PHL 20)

<<<CREATING CB>>> TIME = 0
CREATE-CLOCK ** (SIG CLK) (RATE 1) (PT 2.0) (NT 0.79999999)

<<<DESTROYING CB>>> TIME = 0
CREATE-CLOCK ** (SIG CLK) (RATE 1) (PT 2.0) (NT 0.79999999)

<<<CREATING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG CLK) (CVOLTS 0.19999999) (CRATE 1) (PT 2.0) (NT
 0.79999999) (PLH 0) (PHL 0)

<<<DESTROYING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG CLK) (CVOLTS 0.19999999) (CRATE 1) (PT 2.0) (NT
 0.79999999) (PLH 0) (PHL 0)

COMMAND: *(ADD(ALLOCATE-ACTIVATE CLOCKON CLK 1))


COMMAND: *(DEL(VOLTS IN1 *))


COMMAND: *(ADD(VOLTS IN1 3.4))
```

```
COMMAND: *PICTURE


****TIME****
0
****EXPRS****
(CLOCK CLK LOW)
(SPEED CLK 0)
(PHLIN CLK 0)
(PHLIN IN1 20)
(PHLIN OUT1 0)
(PHLIN OUT2 0)
(PLHIN CLK 0)
(PLHIN IN1 14)
(PLHIN OUT1 0)
(PLHIN OUT2 0)
(PULSEDN CLK OFF)
(PULSEDN IN1 OFF)
(PULSEDN OUT1 OFF)
(PULSEDN OUT2 OFF)
(PULSEUP CLK OFF)
(PULSEUP IN1 OFF)
(PULSEUP OUT1 OFF)
(PULSEUP OUT2 OFF)
(NTHRESH CLK 0.79999999)
(NTHRESH IN1 0.79999999)
(NTHRESH OUT1 0.79999999)
(NTHRESH OUT2 0.79999999)
(PTHRESH CLK 2.0)
(PTHRESH IN1 2.0)
(PTHRESH OUT1 2.0)
(PTHRESH OUT2 2.0)
(RORIN CLK 1)
(RORIN IN1 1)
(RORIN OUT1 1)
(RORIN OUT2 1)
(VOLTS IN1 3.4000000)
(VOLTS CLK 0.19999999)
(VOLTS OUT1 0.19999999)
(VOLTS OUT2 3.4000000)
(TYPE CLK SIGNAL)
(TYPE IN1 SIGNAL)
(TYPE OUT1 SIGNAL)
(TYPE OUT2 SIGNAL)
(STATE OUT1 LOW)
(TUPLE CLK IN1 OUT1 OUT2)
(ALLOCATE-ACTIVATE CLOCKON CLK 1)
****SKLRS****
*****************

COMMAND: *GO


<<<CREATING CB>>> TIME = 0
CLOCKON ** (C CLK) (CSPEED 1)

<<<CREATING CB>>> TIME = 0
LOWCLOCK ** (C CLK) (CSPEED 1) (CVOLTS 0.19999999)
```

```
****TIME****
50
****EXPRS****
(CLOCK CLK LOW)
(SPEED CLK 1)
(PHLIN CLK 0)
(PHLIN IN1 20)
(PHLIN OUT1 0)
(PHLIN OUT2 0)
(PLHIN CLK 0)
(PLHIN IN1 14)
(PLHIN OUT1 0)
(PLHIN OUT2 0)
(PULSEDN CLK OFF)
(PULSEDN IN1 OFF)
(PULSEDN OUT1 OFF)
(PULSEDN OUT2 OFF)
(PULSEUP CLK OFF)
(PULSEUP IN1 OFF)
(PULSEUP OUT1 OFF)
(PULSEUP OUT2 OFF)
(NTHRESH CLK 0.79999999)
(NTHRESH IN1 0.79999999)
(NTHRESH OUT1 0.79999999)
(NTHRESH OUT2 0.79999999)
(PTHRESH CLK 2.0)
(PTHRESH IN1 2.0)
(PTHRESH OUT1 2.0)
(PTHRESH OUT2 2.0)
(RORIN CLK 1)
(RORIN IN1 1)
(RORIN OUT1 1)
(RORIN OUT2 1)
(VOLTS IN1 3.4000000)
(VOLTS CLK 0.19999999)
(VOLTS OUT1 0.19999999)
(VOLTS OUT2 3.4000000)
(TYPE CLK SIGNAL)
(TYPE IN1 SIGNAL)
(TYPE OUT1 SIGNAL)
(TYPE OUT2 SIGNAL)
(STATE OUT1 LOW)
(TUPLE CLK IN1 OUT1 OUT2)
(ALLOCATE-ACTIVATE CLOCKON CLK 1)
****SKLRS****
**********

<<<DESTROYING CB>>> TIME = 500.0
LOWCLOCK ** (C CLK) (CSPEED 1) (CVOLTS 0.19999999)

<<<CREATING CB>>> TIME = 500.0
STARTUP ** (S CLK) (CVOLTS 0.19999999) (CRORIN 1) (CPTHRESH 2.0)

<<<DESTROYING CB>>> TIME = 501.79999
STARTUP ** (S CLK) (CVOLTS 0.19999999) (CRORIN 1) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 501.79999
FINISHUP ** (S CLK) (CVOLTS 2.0) (CRORIN 1) (CPTHRESH 2.0)
```

```
<<<CREATING CB>>> TIME = 501.79999
FFOUTHIGH ** (CLK1 CLK) (DIN IN1) (Q OUT1) (QNOT OUT2) (CDIN 3.400000
0) (CQ 0.19999999) (CQNOT 3.4000000)

<<<DESTROYING CB>>> TIME = 501.79999
FFOUTHIGH ** (CLK1 CLK) (DIN IN1) (Q OUT1) (QNOT OUT2) (CDIN 3.400000
0) (CQ 0.19999999) (CQNOT 3.4000000)

<<<CREATING CB>>> TIME = 501.79999
PROPDELAYLH ** (Q IN1) (L OUT1) (CPLHIN 14) (CRORIN 1) (CVOLTS 0.1999
9999) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 501.79999
PROPDELAYHL ** (Q IN1) (Z OUT2) (CPHLIN 20) (CRORIN 1) (CVOLTS 3.4000
000) (CNTHRESH 0.79999999)

****TIME****
502
****EXPRS****
(CLOCK CLK HIGH)
(SPEED CLK 1)
(PHLIN CLK 0)
(PHLIN IN1 20)
(PHLIN OUT1 0)
(PHLIN OUT2 0)
(PLHIN CLK 0)
(PLHIN IN1 14)
(PLHIN OUT1 0)
(PLHIN OUT2 0)
(PULSEDN CLK OFF)
(PULSEDN IN1 OFF)
(PULSEDN OUT1 OFF)
(PULSEDN OUT2 OFF)
(PULSEUP CLK ON)
(PULSEUP IN1 OFF)
(PULSEUP OUT1 OFF)
(PULSEUP OUT2 OFF)
(NTHRESH CLK 0.79999999)
(NTHRESH IN1 0.79999999)
(NTHRESH OUT1 0.79999999)
(NTHRESH OUT2 0.79999999)
(PTHRESH CLK 2.0)
(PTHRESH IN1 2.0)
(PTHRESH OUT1 2.0)
(PTHRESH OUT2 2.0)
(RORIN CLK 1)
(RORIN IN1 1)
(RORIN OUT1 1)
(RORIN OUT2 1)
(VOLTS IN1 3.4000000)
(VOLTS OUT1 0.19999999)
(VOLTS OUT2 3.4000000)
(TYPE CLK SIGNAL)
(TYPE IN1 SIGNAL)
(TYPE OUT1 SIGNAL)
(TYPE OUT2 SIGNAL)
(STATE OUT1 HIGH)
(TUPLE CLK IN1 OUT1 OUT2)
(ALLOCATE-ACTIVATE CLOCKON CLK 1)
****SKLRS****
(VOLTS CLK 2.2000007)
**********
```

```
<<<DESTROYING CB>>> TIME = 503.20000
FINISHUP ** (S CLK) (CVOLTS 2.0) (CRORIN 1) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 503.20000
HIGHCLOCK ** (C CLK) (CSPEED 1) (CVOLTS 3.4000015)

****TIME****
510
****EXPRS****
(CLOCK CLK HIGH)
(SPEED CLK 1)
(PHLIN CLK 0)
(PHLIN IN1 20)
(PHLIN OUT1 0)
(PHLIN OUT2 0)
(PLHIN CLK 0)
(PLHIN IN1 14)
(PLHIN OUT1 0)
(PLHIN OUT2 0)
(PULSEDN CLK OFF)
(PULSEDN IN1 OFF)
(PULSEDN OUT1 OFF)
(PULSEDN OUT2 OFF)
(PULSEUP CLK OFF)
(PULSEUP IN1 OFF)
(PULSEUP OUT1 OFF)
(PULSEUP OUT2 OFF)
(NTHRESH CLK 0.79999999)
(NTHRESH IN1 0.79999999)
(NTHRESH OUT1 0.79999999)
(NTHRESH OUT2 0.79999999)
(PTHRESH CLK 2.0)
(PTHRESH IN1 2.0)
(PTHRESH OUT1 2.0)
(PTHRESH OUT2 2.0)
(RORIN CLK 1)
(RORIN IN1 1)
(RORIN OUT1 1)
(RORIN OUT2 1)
(VOLTS CLK 3.4000015)
(VOLTS IN1 3.4000000)
(VOLTS OUT1 0.19999999)
(VOLTS OUT2 3.4000000)
(TYPE CLK SIGNAL)
(TYPE IN1 SIGNAL)
(TYPE OUT1 SIGNAL)
(TYPE OUT2 SIGNAL)
(STATE OUT1 HIGH)
(TUPLE CLK IN1 OUT1 OUT2)
(ALLOCATE-ACTIVATE CLOCKON CLK 1)
****SKLRS****
**********

<<<DESTROYING CB>>> TIME = 514.0
PROPDELAYLH ** (Q IN1) (L OUT1) (CPLHIN 14) (CRORIN 1) (CVOLTS 0.1999
9999) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 514.0
STARTUP ** (S OUT1) (CVOLTS 0.19999999) (CRORIN 1) (CPTHRESH 2.0)
```

```
<<<DESTROYING CB>>> TIME = 515.80000
STARTUP ** (S OUT1) (CVOLTS 0.19999999) (CRORIN 1) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 515.80000
FINISHUP ** (S OUT1) (CVOLTS 2.0) (CRORIN 1) (CPTHRESH 2.0)

<<<DESTROYING CB>>> TIME = 517.20000
FINISHUP ** (S OUT1) (CVOLTS 2.0) (CRORIN 1) (CPTHRESH 2.0)

<<<DESTROYING CB>>> TIME = 519.19999
PROPDELAYHL ** (Q IN1) (Z OUT2) (CPHLIN 20) (CRORIN 1) (CVOLTS 3.4000
000) (CNTHRESH 0.79999999)

<<<CREATING CB>>> TIME = 519.19999
STARTDN ** (S OUT2) (CVOLTS 3.4000000) (CRORIN 1) (CNTHRESH 0.7999999
9)

<<<DESTROYING CB>>> TIME = 521.79999
STARTDN ** (S OUT2) (CVOLTS 3.4000000) (CRORIN 1) (CNTHRESH 0.7999999
9)

<<<CREATING CB>>> TIME = 521.79999
FINISHDN ** (S OUT2) (CVOLTS 0.79999999) (CRORIN 1) (CNTHRESH 0.79999
999)

<<<DESTROYING CB>>> TIME = 522.39999
FINISHDN ** (S OUT2) (CVOLTS 0.79999999) (CRORIN 1) (CNTHRESH 0.79999
999)

****TIME****
550
****EXPRS****
(CLOCK CLK HIGH)
(SPEED CLK 1)
(PHLIN CLK 0)
(PHLIN IN1 20)
(PHLIN OUT1 0)
(PHLIN OUT2 0)
(PLHIN CLK 0)
(PLHIN IN1 14)
(PLHIN OUT1 0)
(PLHIN OUT2 0)
(PULSEDN CLK OFF)
(PULSEDN IN1 OFF)
(PULSEDN OUT1 OFF)
(PULSEDN OUT2 OFF)
(PULSEUP CLK OFF)
(PULSEUP IN1 OFF)
(PULSEUP OUT1 OFF)
(PULSEUP OUT2 OFF)
(PULSEDN CLK OFF)
(PULSEDN IN1 OFF)
(PULSEDN OUT1 OFF)
(PULSEDN OUT2 OFF)
(NTHRESH CLK 0.79999999)
(NTHRESH IN1 0.7999999)
(NTHRESH OUT1 0.79999999)
(NTHRESH OUT2 0.79999999)
(PTHRESH CLK 2.0)
(PTHRESH IN1 2.0)
```

```
(PTHRESH OUT1 2.0)
(PTHRESH OUT2 2.0)
(RORIN CLK 1)
(RORIN IN1 1)
(RORIN OUT1 1)
(RORIN OUT2 1)
(VOLTS CLK 3.4000000)
(VOLTS IN1 3.4000000)
(VOLTS OUT1 3.4000000)
(VOLTS OUT2 0.19999999)
(TYPE CLK SIGNAL)
(TYPE IN1 SIGNAL)
(TYPE OUT1 SIGNAL)
(TYPE OUT2 SIGNAL)
(STATE OUT1 HIGH)
(TUPLE CLK IN1 OUT1 OUT2)
(ALLOCATE-ACTIVATE CLOCKON CLK 1)
****SKLRS****
*****************

==========================
>>>BREAK AT 800
==========================

COMMAND: *(DEL(ALLOCATE-ACTIVATE * * *))


<<<DESTROYING CB>>> TIME = 800
CLOCKON ** (C CLK) (CSPEED 1)

COMMAND: *GO

==========================


<<<DESTROYING CB>>> TIME = 1003.2000
HIGHCLOCK ** (C CLK) (CSPEED 1) (CVOLTS 3.4000015)

<<<CREATING CB>>> TIME = 1003.2000
STARTDN ** (S CLK) (CVOLTS 3.4000015) (CRORIN 1) (CNTHRESH 0.79999999
)

<<<DESTROYING CB>>> TIME = 1005.8000
STARTDN ** (S CLK) (CVOLTS 3.4000015) (CRORIN 1) (CNTHRESH 0.79999999
)

<<<CREATING CB>>> TIME = 1005.8000
FINISHDN ** (S CLK) (CVOLTS 0.79999999) (CRORIN 1) (CNTHRESH 0.799999
99)

<<<DESTROYING CB>>> TIME = 1006.4000
FINISHDN ** (S CLK) (CVOLTS 0.79999999) (CRORIN 1) (CNTHRESH 0.799999
99)

COMMAND: *STOP

(****TERMINATED-AT-TIME**** 1006.4000)
```

5.

In the previous sections, we have developed models of electronic signals, and of the actions of a clock and a flip-flop. The clock and the flip-flop were developed primarily as learning tools, in order to organize the development of the simultaneous models to follow. The concepts of propagation delay and of voltage transition, and the scenarios implementing these concepts (Table 5.1) are important components of the switch debouncer and of the one-shot, and should be thoroughly understood before continuing.

SCENARIO	FIGURE
STARTUP	1.2
FINISHUP	1.2
STARTDN	1.3
FINISHDN	1.3
PROPDELAYLH	3.1
PROPDELAYHL	3.1

Table 5.1

6. The Switch World

The mechanical switch, which is a common component in digital devices, does not present a clean transition from on to off or from off to on. Instead, the switch "bounces" between contact and out of contact many times (often for several milliseconds) after it is opened or closed. This behavior is unsuitable for digital circuits, which may respond in microseconds, or even in nanoseconds. [7]

The model of a mechanical switch operates as follows. The CREATE-SWITCH scenario (Figure 6.1) creates an initial

```
.1 (CREATE-SWITCH(PAR S R PLH PHL SWITCH)
.2    (ICS(ALLOCATE-ACTIVATE CREATE-SWITCH S R PLH PHL SWITCH))
.3    (EID(ALLOCATE-ACTIVATE CREATE-SWITCH S R PLH PHL SWITCH))
.4    (EIA(ALLOCATE-ACTIVATE CREATE-SIGNAL S 0.2 10 2.0 0.8 PLH PHL)
.5        (ALLOCATE-ACTIVATE CREATE-SIGNAL R 3.4 10 2.0 0.8 PLH PHL)
.6        (DOWN R S SWITCH)
.7        (CONTACT R ON)
.8        (CONTACT S OFF)
.9        (NBOUNCE R 0)(NBOUNCE S 0)))
```

Figure 6.1

SWM with two switch signals, S and R. S is initially low, 0.2 volts, with a transition rate of ten volts per nanosecond, while R is initially high, 3.4 volts, with the same transition rate (lines 6.1.4, 6.1.5). The switch is down (line 6.1.6), R is in contact with the switch (line 6.1.7), S is not in contact with the switch (line 6.1.8), and the switch is not bouncing (line 6.1.9). After an ALLOCATE-ACTIVATE SWITCHUP or SWITCHDN order is found in the SWM, the switch process is initiated. SWITCHUP will be used as a design example.

The SWITCHUP scenario (Figure 6.2) then deletes the current condition of the switch (line 6.2.3), adds the opposite condition (line 6.2.5), and also adds the condition that the switch is bouncing (line 6.2.7). The scenario adds (NBOUNCE S 5), (6.2.7), signifying that the switch will bounce five times. We have chosen to model far fewer bounces than an actual switch would have. The effects of this choice on the other components of the model, however, are the same as a switch which bounces longer.

```
.1 (SWITCHUP (PAR R S T)
.2     (ICS (DOWN R S T)(ALLOCATE-ACTIVATE SWITCHUP T))
.3     (EID (DOWN R S T)(ALLOCATE-ACTIVATE SWITCHUP T)
.4          (CONTACT R *)(CONTACT S *)
.5          (NBOUNCE R *)(NBOUNCE S *))
.6     (EIA (UP R S T)(CONTACT R OFF)(CONTACT S ON)
.7          (NBOUNCE R 0)(NBOUNCE S 5)
.8          (EDGE R DN)(EDGE S UP)))

.9 (SWITCHDN (PAR R S T)
.10    (ICS (UP R S T)(ALLOCATE-ACTIVATE SWITCHDN T))
.11    (EID (UP R S T)(ALLOCATE-ACTIVATE SWITCHDN T)
.12         (NBOUNCE R *)(NBOUNCE S *))
.13.   (EIA (DOWN R S T)(CONTACT R ON)(CONTACT S OFF)
.14         (NBOUNCE R 5)(NBOUNCE S 0)
.15         (EDGE R UP)(EDGE S DN)))
```

Figure 6.2

The STARTUP scenario is initiated by the EDGE condition, and the PULSEUP relation initiates HIT and BOUNCE (Figures 6.3 and 6.4). Each time the rising signal reaches the threshold voltage with the symbolic condition S ON, and the number of bounces left is greater than zero, HIT holds the signal S high for thirty nanoseconds (6.3.7), then changes S to OFF (6.3.8), and starts a negative-going edge for S (6.3.8).

This edge initiates STARTDN, and then BOUNCE takes control. BOUNCE holds S OFF for a time related to the total number of bounces (6.4.6), where each successive initiation of BOUNCE covers a smaller time interval. The switch will continue to hit and bounce, with each hit lasting thirty nanoseconds, and each bounce being shorter, until the output SET is a constant high voltage.

```
.1 (BOUNCE (PAR S  CNBOUNCE)
.2    (ICS  (CONTACT S OFF)(TYPE S SIGNAL)
.3          (NBOUNCE S CNBOUNCE)(PULSEDN S ON))
.4    (ICN  (GT CNBOUNCE 0))
.5    (CCS  (NBOUNCE S CNBOUNCE ))
.6    (CCN  FUNC (*PLUS % (PROG2 (SETQ NEW (SUB1 CNBOUNCE))CNBOUNCE)))
.7    (EPD  (CONTACT S OFF)(NBOUNCE S *))
.8    (EPA  (CONTACT S ON)(NBOUNCE S NEW)(EDGE S UP)))
```

Figure 6.3

```
.1 (HIT (PAR S CNBOUNCE)
.2    (ICS (TYPE S SIGNAL)(CONTACT S ON)
.3         (NBOUNCE S CNBOUNCE)(PULSEUP S ON))
.4    (ICN (GT CNBOUNCE 0))
.5    (CCS (NBOUNCE S CNBOUNCE))
.6    (CCN FUNC (*PLUS % 30))
.7    (EPD (CONTACT S ON))
.8    (EPA (CONTACT S OFF)(EDGE S DN)))
```

Figure 6.4

Example 4 demonstrates the operation of the mechanical switch simulation. After the SWM is created, switch input R is on, and input S is off. The switch is then turned on, and it has five bounces left. HIT is destroyed after 30 nanoseconds, the signal begins a downward transition, and R and S are off at time = 33. The switch then continues to hit and bounce until time = 163.58, when NBOUNCE S = 0, S is ON and R is OFF.

```
*(HSIM)

==========================
HENDRIX SIMULATION SYSTEM
==========================

INPUT SCENARIO LIST: *(EVAL SLIST)

STARTUP FINISHUP STARTDN FINISHDN HIT BOUNCE SWITCHUP
SWITCHDN CREATE-SIGNAL CREATE-SWITCH

INPUT SWM RELATION LIST: *(EVAL SWM)


COMMAND: *(TRACE *)


COMMAND: *(SNAPSHOTS 20 33)


COMMAND: *(ADD(ALLOCATE-ACTIVATE CREATE-SWITCH S R 0 0 SW1))


COMMAND: *GO


<<<CREATING CB>>> TIME = 0
CREATE-SWITCH ** (S S) (R R) (PLH 0) (PHL 0) (SWITCH SW1)

<<<DESTROYING CB>>> TIME = 0
CREATE-SWITCH ** (S S) (R R) (PLH 0) (PHL 0) (SWITCH SW1)

<<<CREATING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG R) (CVOLTS 3.4000000) (CRATE 10) (PT 2.0) (NT 0
.79999999) (PLH 0) (PHL 0)

<<<DESTROYING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG R) (CVOLTS 3.4000000) (CRATE 10) (PT 2.0) (NT 0
.79999999) (PLH 0) (PHL 0)

<<<CREATING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG S) (CVOLTS 0.19999999) (CRATE 10) (PT 2.0) (NT
0.79999999) (PLH 0) (PHL 0)

<<<DESTROYING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG S) (CVOLTS 0.19999999) (CRATE 10) (PT 2.0) (NT
0.79999999) (PLH 0) (PHL 0)

COMMAND: *(ADD(ALLOCATE-ACTIVATE SWITCHUP SW1))


COMMAND: *GO


<<<CREATING CB>>> TIME = 0
SWITCHUP ** (R R) (S S) (T SW1)

<<<DESTROYING CB>>> TIME = 0
SWITCHUP ** (R R) (S S) (T SW1)
```

```
<<<CREATING CB>>> TIME = 0
STARTUP ** (S S) (CVOLTS 0.19999999) (CRORIN 10) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 0
STARTDN ** (S R) (CVOLTS 3.4000000) (CRORIN 10) (CNTHRESH 0.79999999)


<<<DESTROYING CB>>> TIME = 0.17999999
STARTUP ** (S S) (CVOLTS 0.19999999) (CRORIN 10) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 0.17999999
FINISHUP ** (S S) (CVOLTS 2.0) (CRORIN 10) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 0.17999999
HIT ** (S S) (CNBOUNCE 5)

<<<DESTROYING CB>>> TIME = 0.26000000
STARTDN ** (S R) (CVOLTS 3.4000000) (CRORIN 10) (CNTHRESH 0.79999999)


<<<CREATING CB>>> TIME = 0.26000000
FINISHDN ** (S R) (CVOLTS 0.79999999) (CRORIN 10) (CNTHRESH 0.7999999
9)

<<<DESTROYING CB>>> TIME = 0.32000000
FINISHDN ** (S R) (CVOLTS 0.79999999) (CRORIN 10) (CNTHRESH 0.7999999
9)

<<<DESTROYING CB>>> TIME = 0.32000000
FINISHUP ** (S S) (CVOLTS 2.0) (CRORIN 10) (CPTHRESH 2.0)

****TIME****
20
****EXPRS****
(UP R S SW1)
(PHLIN S 0)
(PHLIN R 0)
(PLHIN S 0)
(PLHIN R 0)
(PULSEDN R OFF)
(PULSEDN S OFF)
(PULSEUP S OFF)
(PULSEUP R OFF)
(NTHRESH S 0.79999999)
(NTHRESH R 0.79999999)
(PTHRESH S 2.0)
(PTHRESH R 2.0)
(RORIN S 10)
(RORIN R 10)
(VOLTS S 3.4000000)
(VOLTS R 0.20000001)
(TYPE S SIGNAL)
(TYPE R SIGNAL)
(NBOUNCE S 5)
(NBOUNCE R 0)
(CONTACT S ON)
(CONTACT R OFF)
****SKLRS****
**********
```

```
<<<DESTROYING CB>>> TIME = 30.180000
HIT ** (S S) (CNBOUNCE 5)

<<<CREATING CB>>> TIME = 30.180000
STARTDN ** (S S) (CVOLTS 3.4000000) (CRORIN 10) (CNTHRESH 0.79999999)


<<<DESTROYING CB>>> TIME = 30.440000
STARTDN ** (S S) (CVOLTS 3.4000000) (CRORIN 10) (CNTHRESH 0.79999999)


<<<CREATING CB>>> TIME = 30.440000
FINISHDN ** (S S) (CVOLTS 0.79999999) (CRORIN 10) (CNTHRESH 0.7999999
9)

<<<CREATING CB>>> TIME = 30.440000
BOUNCE ** (S S) (CNBOUNCE 5)

<<<DESTROYING CB>>> TIME = 30.5
FINISHDN ** (S S) (CVOLTS 0.79999999) (CRORIN 10) (CNTHRESH 0.7999999
9)

****TIME****
33
****EXPRS****
(UP R S SW1)
(PHLIN S 0)
(PHLIN R 0)
(PLHIN S 0)
(PLHIN R 0)
(PULSEDN S OFF)
(PULSEDN R OFF)
(PULSEUP S OFF)
(PULSEUP R OFF)
(NTHRESH S 0.79999999)
(NTHRESH R 0.79999999)
(PTHRESH S 2.0)
(PTHRESH R 2.0)
(RORIN S 10)
(RORIN R 10)
(VOLTS S 0.20000056)
(VOLTS R 0.20000001)
(TYPE S SIGNAL)
(TYPE R SIGNAL)
(NBOUNCE S 5)
(NBOUNCE R 0)
(CONTACT S OFF)
(CONTACT R OFF)
****SKLRS****
**********************

<<<DESTROYING CB>>> TIME = 35.440000
BOUNCE ** (S S) (CNBOUNCE 5)

<<<CREATING CB>>> TIME = 35.440000
STARTUP ** (S S) (CVOLTS 0.20000056) (CRORIN 10) (CPTHRESH 2.0)

<<<DESTROYING CB>>> TIME = 35.619999
STARTUP ** (S S) (CVOLTS 0.20000056) (CRORIN 10) (CPTHRESH 2.0)
```

```
<<<CREATING CB>>> TIME = 35.619999
FINISHUP ** (S S) (CVOLTS 2.0) (CRORIN 10) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 35.619999
HIT ** (S S) (CNBOUNCE NEW)

<<<DESTROYING CB>>> TIME = 35.759999
FINISHUP ** (S S) (CVOLTS 2.0) (CRORIN 10) (CPTHRESH 2.0)

<<<DESTROYING CB>>> TIME = 65.619999
HIT ** (S S) (CNBOUNCE NEW)

<<<CREATING CB>>> TIME = 65.619999
STARTDN ** (S S) (CVOLTS 3.3999986) (CRORIN 10) (CNTHRESH 0.79999999)


<<<DESTROYING CB>>> TIME = 65.880000
STARTDN ** (S S) (CVOLTS 3.3999986) (CRORIN 10) (CNTHRESH 0.79999999)


<<<CREATING CB>>> TIME = 65.880000
FINISHDN ** (S S) (CVOLTS 0.79999999) (CRORIN 10) (CNTHRESH 0.7999999
9)

<<<CREATING CB>>> TIME = 65.880000
BOUNCE ** (S S) (CNBOUNCE NEW)

<<<DESTROYING CB>>> TIME = 65.940000
FINISHDN ** (S S) (CVOLTS 0.79999999) (CRORIN 10) (CNTHRESH 0.7999999
9)

<<<DESTROYING CB>>> TIME = 68.880000
BOUNCE ** (S S) (CNBOUNCE NEW)

<<<CREATING CB>>> TIME = 68.880000
STARTUP ** (S S) (CVOLTS 0.19999580) (CRORIN 10) (CPTHRESH 2.0)

<<<DESTROYING CB>>> TIME = 69.060000
STARTUP ** (S S) (CVOLTS 0.19999580) (CRORIN 10) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 69.060000
FINISHUP ** (S S) (CVOLTS 2.0) (CRORIN 10) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 69.060000
HIT ** (S S) (CNBOUNCE NEW)

<<<DESTROYING CB>>> TIME = 69.200000
FINISHUP ** (S S) (CVOLTS 2.0) (CRORIN 10) (CPTHRESH 2.0)

<<<DESTROYING CB>>> TIME = 99.060000
HIT ** (S S) (CNBOUNCE NEW)

<<<CREATING CB>>> TIME = 99.060000
STARTDN ** (S S) (CVOLTS 3.4000034) (CRORIN 10) (CNTHRESH 0.79999999)


<<<DESTROYING CB>>> TIME = 99.320000
STARTDN ** (S S) (CVOLTS 3.4000034) (CRORIN 10) (CNTHRESH 0.79999999)
```

```
<<<CREATING CB>>> TIME = 99.320000
FINISHDN ** (S S) (CVOLTS 0.79999999) (CRORIN 10) (CNTHRESH 0.7999999
9)

<<<CREATING CB>>> TIME = 99.320000
BOUNCE ** (S S) (CNBOUNCE NEW)

<<<DESTROYING CB>>> TIME = 99.380001
FINISHDN ** (S S) (CVOLTS 0.79999999) (CRORIN 10) (CNTHRESH 0.7999999
9)

<<<DESTROYING CB>>> TIME = 101.32000
BOUNCE ** (S S) (CNBOUNCE NEW)

<<<CREATING CB>>> TIME = 101.32000
STARTUP ** (S S) (CVOLTS 0.19999580) (CRORIN 10) (CPTHRESH 2.0)

<<<DESTROYING CB>>> TIME = 101.50000
STARTUP ** (S S) (CVOLTS 0.19999580) (CRORIN 10) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 101.50000
FINISHUP ** (S S) (CVOLTS 2.0) (CRORIN 10) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 101.50000
HIT ** (S S) (CNBOUNCE NEW)

<<<DESTROYING CB>>> TIME = 101.64000
FINISHUP ** (S S) (CVOLTS 2.0) (CRORIN 10) (CPTHRESH 2.0)

<<<DESTROYING CB>>> TIME = 131.50000
HIT ** (S S) (CNBOUNCE NEW)

<<<CREATING CB>>> TIME = 131.50000
STARTDN ** (S S) (CVOLTS 3.4000034) (CRORIN 10) (CNTHRESH 0.79999999)


<<<DESTROYING CB>>> TIME = 131.76000
STARTDN ** (S S) (CVOLTS 3.4000034) (CRORIN 10) (CNTHRESH 0.79999999)


<<<CREATING CB>>> TIME = 131.76000
FINISHDN ** (S S) (CVOLTS 0.79999999) (CRORIN 10) (CNTHRESH 0.7999999
9)

<<<CREATING CB>>> TIME = 131.76000
BOUNCE ** (S S) (CNBOUNCE NEW)

<<<DESTROYING CB>>> TIME = 131.82000
FINISHDN ** (S S) (CVOLTS 0.79999999) (CRORIN 10) (CNTHRESH 0.7999999
9)

<<<DESTROYING CB>>> TIME = 132.76000
BOUNCE ** (S S) (CNBOUNCE NEW)

<<<CREATING CB>>> TIME = 132.76000
STARTUP ** (S S) (CVOLTS 0.20000533) (CRORIN 10) (CPTHRESH 2.0)

<<<DESTROYING CB>>> TIME = 132.94000
STARTUP ** (S S) (CVOLTS 0.20000533) (CRORIN 10) (CPTHRESH 2.0)
```

```
<<<CREATING CB>>> TIME = 132.94000
FINISHUP ** (S S) (CVOLTS 2.0) (CRORIN 10) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 132.94000
HIT ** (S S) (CNBOUNCE NEW)

<<<DESTROYING CB>>> TIME = 133.08000
FINISHUP ** (S S) (CVOLTS 2.0) (CRORIN 10) (CPTHRESH 2.0)

<<<DESTROYING CB>>> TIME = 162.94000
HIT ** (S S) (CNBOUNCE NEW)

<<<CREATING CB>>> TIME = 162.94000
STARTDN ** (S S) (CVOLTS 3.3999938) (CRORIN 10) (CNTHRESH 0.79999999)


<<<DESTROYING CB>>> TIME = 163.20000
STARTDN ** (S S) (CVOLTS 3.3999938) (CRORIN 10) (CNTHRESH 0.79999999)


<<<CREATING CB>>> TIME = 163.20000
FINISHDN ** (S S) (CVOLTS 0.79999999) (CRORIN 10) (CNTHRESH 0.7999999
9)

<<<CREATING CB>>> TIME = 163.20000
BOUNCE ** (S S) (CNBOUNCE NEW)

<<<DESTROYING CB>>> TIME = 163.20000
BOUNCE ** (S S) (CNBOUNCE NEW)

<<<DESTROYING CB>>> TIME = 163.26000
FINISHDN ** (S S) (CVOLTS 0.79999999) (CRORIN 10) (CNTHRESH 0.7999999
9)

<<<CREATING CB>>> TIME = 163.26000
STARTUP ** (S S) (CVOLTS 0.20000533) (CRORIN 10) (CPTHRESH 2.0)

<<<DESTROYING CB>>> TIME = 163.44000
STARTUP ** (S S) (CVOLTS 0.20000533) (CRORIN 10) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 163.44000
FINISHUP ** (S S) (CVOLTS 2.0) (CRORIN 10) (CPTHRESH 2.0)

<<<DESTROYING CB>>> TIME = 163.58000
FINISHUP ** (S S) (CVOLTS 2.0) (CRORIN 10) (CPTHRESH 2.0)

COMMAND: *PICTURE
```

```
****TIME****
163.58000
****EXPRS****
(UP R S SW1)
(PHLIN S 0)
(PHLIN R 0)
(PLHIN S 0)
(PLHIN R 0)
(PULSEDN S OFF)
(PULSEDN R OFF)
(PULSEUP S OFF)
(PULSEUP R OFF)
(NTHRESH S 0.79999999)
(NTHRESH R 0.79999999)
(PTHRESH S 2.0)
(PTHRESH R 2.0)
(RORIN S 10)
(RORIN R 10)
(VOLTS S 3.3999938)
(VOLTS R 0.20000001)
(TYPE S SIGNAL)
(TYPE R SIGNAL)
(NBOUNCE S NEW)
(NBOUNCE R 0)
(CONTACT S ON)
(CONTACT R OFF)
****SKLRS****
******************

COMMAND: *STOP

(****TERMINATED-AT-TIME**** 163.58000)
```

7. The Debounced Switch

A switch debouncer is a circuit which only responds to the first change in voltage from a mechanical switch, ignoring subsequent fluctuations. On the MSI level, a switch debouncer may be constructed from an R-S (master-slave) flip-flop, while on the SSI level, a pair of cross-coupled NOR or NAND gates produce a debounced output. We have chosen to model the SSI circuit shown in Figure 7.1. [7,p.12-31]

The first step when simulating a logic circuit is to determine the truth table for each type of gate in the circuit. The truth table for a 7402 NOR gate is: [6,p.5-22]

IN1	IN2	OUT
L	L	H
L	H	L
H	L	L
H	H	L

The programmer should then write a scenario for each line of the truth table (Figure 7.2). The scenario HIGH7402 will be used as an example. The ICS for the scenario will include a tuple showing the two imputs and the output (7.2.2), the voltage levels of the inputs and output (7.2.3), and the state (high or low) of the output (7.2.2). The ICN (7.2.5-7.2.7) contain the voltage boundaries necessary to initiate each process. The scenario will then delete the current state of the output (7.2.8), add the new state (7.2.9), and start the propagation delay/signal change process (7.2.9).

The SWM for the debouncer is created by CREATE-DEBOUNCE, Figure 7.3. The debouncer has two outputs, OH and OL (7.3.2), and a switch SWITCH. A CREATE-SWITCH order is added to the

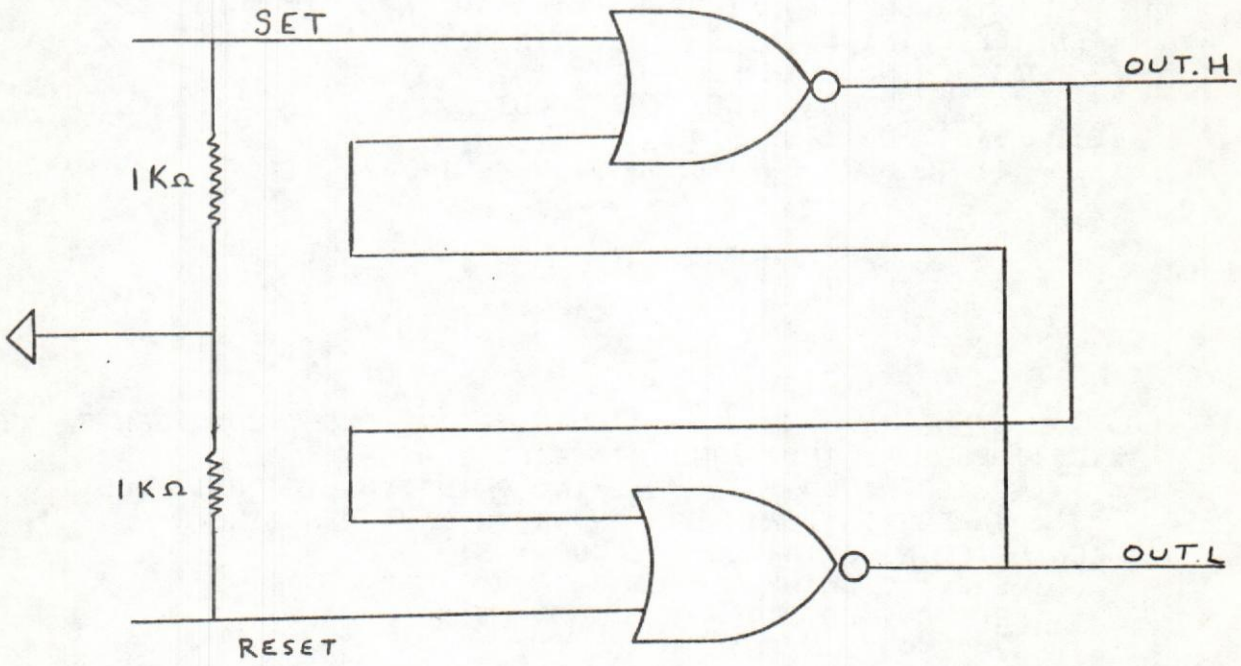


Figure 7.1

```
.1  (HIGH7402 (PAR IN1 IN2 OUT1 : CVIN1 CVIN2 CVOUT CPTHRESH CNTHRESH)
.2     (ICS (TUPLE IN1 IN2 OUT1)(STATE OUT1 LOW)
.3          (VOLTS IN1 CVIN1)(VOLTS IN2 CVIN2)(VOLTS OUT1 CVOUT)
.4          (PTHRESH OUT1 CPTHRESH)(NTHRESH IN1 CNTHRESH))
.5     (ICN (LE CVIN1 CNTHRESH)(GE CVIN1 0)
.6          (LE CVIN2 CNTHRESH)(GE CVIN2 0)
.7          (LE CVOUT CPTHRESH)(GE CVOUT 0))
.8     (EID (STATE OUT1 LOW))
.9     (EIA (STATE OUT1 HIGH)(TRIGLH IN1 OUT1)))
```

```
(LOW7402-1 (PAR IN1 IN2 OUT1 : CVIN1 CVIN2 CVOUT CPTHRESH CNTHRESH)
   (ICS (TUPLE IN1 IN2 OUT1)(STATE OUT1 HIGH)
        (VOLTS IN1 CVIN1)(VOLTS IN2 CVIN2)(VOLTS OUT1 CVOUT)
        (NTHRESH IN1 CNTHRESH)(PTHRESH IN2 CPTHRESH))
   (ICN (LE CVIN1 CNTHRESH)(GE CVIN1 0)
        (GE CVIN2 CPTHRESH)(LE CVIN2 5.0)
        (GE CVOUT CNTHRESH)(LE CVOUT 5.0))
   (EID (STATE OUT1 HIGH))
   (EIA (STATE OUT1 LOW)(TRIGHL IN1 OUT1)))
```

```
(LOW7402-2(PAR IN1 IN2 OUT1 : CVIN1 CVIN2 CVOUT CNTHRESH CPTHRESH)
   (ICS(TUPLE IN1 IN2 OUT1)(STATE OUT1 HIGH)
       (VOLTS IN1 CVIN1)(VOLTS IN2 CVIN2)(VOLTS OUT1 CVOUT)
       (PTHRESH IN1 CPTHRESH)(NTHRESH IN2 CNTHRESH))
   (ICN(GE CVIN1 CPTHRESH)(LE CVIN1 5)
       (LE CVIN2 CNTHRESH)(GE CVIN2 0)
       (GE CVOUT CNTHRESH)(LE CVOUT 5))
   (EID(STATE OUT1 HIGH))
   (EIA(STATE OUT1 LOW)(TRIGHL IN1 OUT1)))
```

```
(LOW7402-3 (PAR IN1 IN2 OUT : CVIN1 CVIN2 CVOUT CPTHRESH CNTHRESH)
   (ICS (TUPLE IN1 IN2 OUT1)(STATE OUT1 HIGH)
        (VOLTS IN1 CVIN1)(VOLTS IN2 CVIN2)(VOLTS OUT1 CVOUT)
        (NTHRESH OUT1 CNTHRESH)(PTHRESH IN1 CPTHRESH))
   (ICN (GE CVIN1 CPTHRESH)(LE CVIN1 5.0)
        (GE CVIN2 CPTHRESH)(LE CVIN2 5.0)
        (GE CVOUT CNTHRESH)(LE CVOUT 5.0))
   (EID (STATE OUT1 HIGH))
   (EIA (STATE OUT1 LOW)(TRIGHL IN1 OUT1)))
```

Figure 7.2

SWM (7.3.2), as well as two signals (7.3.5,7.3.6). The OL output is low, the OH output is high (7.3.7), and the tuples (7.3.8) show the cross-coupled nature of the two NOR gates.

The sample run of the switch debouncer (Example 5) shows that SW1 is set, the set input voltage bounces, RESET is low, PROPDELAYLH causes OUTH to go high, and PROPDELAYHL causes OUTL to go low. The switch bounces for about 165 nanoseconds (model time), but the OUTH output is constantly high after the first HIT.

```
.1  (CREATE-DEBOUNCE(PAR S R OL OH SWITCH)
.2     (ICS(ALLOCATE-ACTIVATE CREATE-DEBOUNCE S R OL OH SWITCH))
.3     (EID(ALLOCATE-ACTIVATE CREATE-DEBOUNCE S R OL OH SWITCH))
.4     (EIA(ALLOCATE-ACTIVATE CREATE-SWITCH S R 12 8 SWITCH)
.5         (ALLOCATE-ACTIVATE CREATE-SIGNAL OH 3.4 1 2 0.8 0 0)
.6         (ALLOCATE-ACTIVATE CREATE-SIGNAL OL 0.2 1 2 0.8 0 0)
.7         (STATE OL LOW)(STATE OH HIGH)
.8         (TUPLE S OL OH)(TUPLE R OH OL)))
```

Figure 7.3

Example 5 -- The Switch Debouncer

```
*(HSIM)

==========================
HENDRIX SIMULATION SYSTEM
==========================

INPUT SCENARIO LIST: *(EVAL SLIST)

STARTUP FINISHUP STARTDN FINISHDN PROPDELAYLH PROPDELAYHL
HIGH7402 LOW7402-1 LOW7402-2 LOW7402-3 BOUNCE HIT SWITCHUP SWITCHDN
CREATE-SIGNAL CREATE-SWITCH CREATE-DEBOUNCE

INPUT SWM RELATION LIST: *(EVAL SWM)


COMMAND: *(TRACE *)


COMMAND: *(SNAPSHOTS 7 10 20 33)


COMMAND: *(BREAK 36)


COMMAND: *(ADD(ALLOCATE-ACTIVATE CREATE-DEBOUNCE SET RESET OUTL OUTH SW2
))


COMMAND: *GO


<<<CREATING CB>>> TIME = 0
CREATE-DEBOUNCE ** (S SET) (R RESET) (OL OUTL) (OH OUTH) (SWITCH SW2)


<<<DESTROYING CB>>> TIME = 0
CREATE-DEBOUNCE ** (S SET) (R RESET) (OL OUTL) (OH OUTH) (SWITCH SW2)


<<<CREATING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG OUTL) (CVOLTS 0.19999999) (CRATE 1) (PT 2) (NT
0.79999999) (PLH 0) (PHL 0)

<<<DESTROYING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG OUTL) (CVOLTS 0.19999999) (CRATE 1) (PT 2) (NT
0.79999999) (PLH 0) (PHL 0)

<<<CREATING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG OUTH) (CVOLTS 3.4000000) (CRATE 1) (PT 2) (NT 0
.79999999) (PLH 0) (PHL 0)

<<<DESTROYING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG OUTH) (CVOLTS 3.4000000) (CRATE 1) (PT 2) (NT 0
.79999999) (PLH 0) (PHL 0)

<<<CREATING CB>>> TIME = 0
CREATE-SWITCH ** (S SET) (R RESET) (PLH 12) (PHL 8) (SWITCH SW2)
```

```
<<<DESTROYING CB>>> TIME = 0
CREATE-SWITCH ** (S SET) (R RESET) (PLH 12) (PHL 8) (SWITCH SW2)

<<<CREATING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG RESET) (CVOLTS 3.4000000) (CRATE 10) (PT 2.0) (
NT 0.79999999) (PLH 12) (PHL 8)

<<<DESTROYING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG RESET) (CVOLTS 3.4000000) (CRATE 10) (PT 2.0) (
NT 0.79999999) (PLH 12) (PHL 8)

<<<CREATING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG SET) (CVOLTS 0.19999999) (CRATE 10) (PT 2.0) (N
T 0.79999999) (PLH 12) (PHL 8)

<<<DESTROYING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG SET) (CVOLTS 0.19999999) (CRATE 10) (PT 2.0) (N
T 0.79999999) (PLH 12) (PHL 8)

COMMAND: *(ADD(ALLOCATE-ACTIVATE SWITCHUP SW2))


COMMAND: *GO


<<<CREATING CB>>> TIME = 0
SWITCHUP ** (R RESET) (S SET) (T SW2)

<<<DESTROYING CB>>> TIME = 0
SWITCHUP ** (R RESET) (S SET) (T SW2)

<<<CREATING CB>>> TIME = 0
STARTUP ** (S SET) (CVOLTS 0.19999999) (CRORIN 10) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 0
STARTDN ** (S RESET) (CVOLTS 3.4000000) (CRORIN 10) (CNTHRESH 0.79999
999)

<<<DESTROYING CB>>> TIME = 0.17999999
STARTUP ** (S SET) (CVOLTS 0.19999999) (CRORIN 10) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 0.17999999
FINISHUP ** (S SET) (CVOLTS 2.0) (CRORIN 10) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 0.17999999
HIT ** (S SET) (CNBOUNCE 5)

<<<DESTROYING CB>>> TIME = 0.26000000
STARTDN ** (S RESET) (CVOLTS 3.4000000) (CRORIN 10) (CNTHRESH 0.79999
999)

<<<CREATING CB>>> TIME = 0.26000000
FINISHDN ** (S RESET) (CVOLTS 0.79999999) (CRORIN 10) (CNTHRESH 0.799
99999)

<<<DESTROYING CB>>> TIME = 0.32000000
FINISHDN ** (S RESET) (CVOLTS 0.79999999) (CRORIN 10) (CNTHRESH 0.799
99999)

<<<DESTROYING CB>>> TIME = 0.32000000
FINISHUP ** (S SET) (CVOLTS 2.0) (CRORIN 10) (CPTHRESH 2.0)
```

```
<<<CREATING CB>>> TIME = 0.32000000
LOW7402-2 ** (IN1 SET) (IN2 OUTL) (OUT1 OUTH) (CVIN1 3.4000000) (CVIN
2 0.19999999) (CVOUT 3.4000000) (CNTHRESH 0.79999999) (CPTHRESH 2.0)

<<<DESTROYING CB>>> TIME = 0.32000000
LOW7402-2 ** (IN1 SET) (IN2 OUTL) (OUT1 OUTH) (CVIN1 3.4000000) (CVIN
2 0.19999999) (CVOUT 3.4000000) (CNTHRESH 0.79999999) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 0.32000000
PROPDELAYHL ** (Q SET) (Z OUTH) (CPHLIN 8) (CRORIN 1) (CVOLTS 3.40000
00) (CNTHRESH 0.79999999)

<<<DESTROYING CB>>> TIME = 5.7199999
PROPDELAYHL ** (Q SET) (Z OUTH) (CPHLIN 8) (CRORIN 1) (CVOLTS 3.40000
00) (CNTHRESH 0.79999999)

<<<CREATING CB>>> TIME = 5.7199999
STARTDN ** (S OUTH) (CVOLTS 3.4000000) (CRORIN 1) (CNTHRESH 0.7999999
9)

****TIME****
7
****EXPRS****
(UP RESET SET SW2)
(NBOUNCE SET 5)
(NBOUNCE RESET 0)
(CONTACT SET ON)
(CONTACT RESET OFF)
(PHLIN SET 8)
(PHLIN RESET 8)
(PHLIN OUTH 0)
(PHLIN OUTL 0)
(PLHIN SET 12)
(PLHIN RESET 12)
(PLHIN OUTH 0)
(PLHIN OUTL 0)
(PULSEDN RESET OFF)
(PULSEDN SET OFF)
(PULSEDN OUTH OFF)
(PULSEDN OUTL OFF)
(PULSEUP SET OFF)
(PULSEUP RESET OFF)
(PULSEUP OUTH OFF)
(PULSEUP OUTL OFF)
(NTHRESH SET 0.79999999)
(NTHRESH RESET 0.79999999)
(NTHRESH OUTH 0.79999999)
(NTHRESH OUTL 0.79999999)
(PTHRESH SET 2.0)
(PTHRESH RESET 2.0)
(PTHRESH OUTH 2)
(PTHRESH OUTL 2)
(RORIN SET 10)
(RORIN RESET 10)
(RORIN OUTH 1)
(RORIN OUTL 1)
(VOLTS SET 3.4000000)
(VOLTS RESET 0.20000001)
(VOLTS OUTL 0.19999999)
```

```
(TYPE SET SIGNAL)
(TYPE RESET SIGNAL)
(TYPE OUTH SIGNAL)
(TYPE OUTL SIGNAL)
(TUPLE RESET OUTH OUTL)
(TUPLE SET OUTL OUTH)
(STATE OUTH LOW)
(STATE OUTL LOW)
****SKLRS****
(VOLTS OUTH 2.1199999)
****************

<<<DESTROYING CB>>> TIME = 8.3200000
STARTDN ** (S OUTH) (CVOLTS 3.4000000) (CRORIN 1) (CNTHRESH 0.7999999
9)

<<<CREATING CB>>> TIME = 8.3200000
FINISHDN ** (S OUTH) (CVOLTS 0.79999999) (CRORIN 1) (CNTHRESH 0.79999
999)

<<<DESTROYING CB>>> TIME = 8.9200000
FINISHDN ** (S OUTH) (CVOLTS 0.79999999) (CRORIN 1) (CNTHRESH 0.79999
999)

<<<CREATING CB>>> TIME = 8.9200000
HIGH7402 ** (IN1 RESET) (IN2 OUTH) (OUT1 OUTL) (CVIN1 0.20000001) (CV
IN2 0.19999997) (CVOUT 0.19999999) (CPTHRESH 2) (CNTHRESH 0.79999999)


<<<DESTROYING CB>>> TIME = 8.9200000
HIGH7402 ** (IN1 RESET) (IN2 OUTH) (OUT1 OUTL) (CVIN1 0.20000001) (CV
IN2 0.19999997) (CVOUT 0.19999999) (CPTHRESH 2) (CNTHRESH 0.79999999)


<<<CREATING CB>>> TIME = 8.9200000
PROPDELAYLH ** (Q RESET) (L OUTL) (CPLHIN 12) (CRORIN 1) (CVOLTS 0.19
999999) (CPTHRESH 2)

****TIME****
10
****EXPRS****
(UP RESET SET SW2)
(NBOUNCE SET 5)
(NBOUNCE RESET 0)
(CONTACT SET ON)
(CONTACT RESET OFF)
(PHLIN SET 8)
(PHLIN RESET 8)
(PHLIN OUTH 0)
(PHLIN OUTL 0)
(PLHIN SET 12)
(PLHIN RESET 12)
(PLHIN OUTH 0)
(PLHIN OUTL 0)
(PULSEDN OUTH OFF)
(PULSEDN RESET OFF)
(PULSEDN SET OFF)
(PULSEDN OUTL OFF)
(PULSEUP SET OFF)
(PULSEUP RESET OFF)
```

```
(PULSEUP OUTH OFF)
(PULSEUP OUTL OFF)
(NTHRESH SET 0.79999999)
(NTHRESH RESET 0.79999999)
(NTHRESH OUTH 0.79999999)
(NTHRESH OUTL 0.79999999)
(PTHRESH SET 2.0)
(PTHRESH RESET 2.0)
(PTHRESH OUTH 2)
(PTHRESH OUTL 2)
(RORIN SET 10)
(RORIN RESET 10)
(RORIN OUTH 1)
(RORIN OUTL 1)
(VOLTS OUTH 0.19999997)
(VOLTS SET 3.4000000)
(VOLTS RESET 0.20000001)
(VOLTS OUTL 0.19999999)
(TYPE SET SIGNAL)
(TYPE RESET SIGNAL)
(TYPE OUTH SIGNAL)
(TYPE OUTL SIGNAL)
(TUPLE RESET OUTH OUTL)
(TUPLE SET OUTL OUTH)
(STATE OUTL HIGH)
(STATE OUTH LOW)
****SKLRS****
******************

<<<DESTROYING CB>>> TIME = 19.120000
PROPDELAYLH ** (Q RESET) (L OUTL) (CPLHIN 12) (CRORIN 1) (CVOLTS 0.19
999999) (CPTHRESH 2)

<<<CREATING CB>>> TIME = 19.120000
STARTUP ** (S OUTL) (CVOLTS 0.19999999) (CRORIN 1) (CPTHRESH 2)

****TIME****
20
****EXPRS****
(UP RESET SET SW2)
(NBOUNCE SET 5)
(NBOUNCE RESET 0)
(CONTACT SET ON)
(CONTACT RESET OFF)
(PHLIN SET 8)
(PHLIN RESET 8)
(PHLIN OUTH 0)
(PHLIN OUTL 0)
(PLHIN SET 12)
(PLHIN RESET 12)
(PLHIN OUTH 0)
(PLHIN OUTL 0)
(PULSEDN OUTH OFF)
(PULSEDN RESET OFF)
(PULSEDN SET OFF)
(PULSEDN OUTL OFF)
(PULSEUP SET OFF)
(PULSEUP RESET OFF)
(PULSEUP OUTH OFF)
(PULSEUP OUTL OFF)
```

```
(NTHRESH SET 0.79999999)
(NTHRESH RESET 0.79999999)
(NTHRESH OUTH 0.79999999)
(NTHRESH OUTL 0.79999999)
(PTHRESH SET 2.0)
(PTHRESH RESET 2.0)
(PTHRESH OUTH 2)
(PTHRESH OUTL 2)
(RORIN SET 10)
(RORIN RESET 10)
(RORIN OUTH 1)
(RORIN OUTL 1)
(VOLTS OUTH 0.19999997)
(VOLTS SET 3.4000000)
(VOLTS RESET 0.20000001)
(TYPE SET SIGNAL)
(TYPE RESET SIGNAL)
(TYPE OUTH SIGNAL)
(TYPE OUTL SIGNAL)
(TUPLE RESET OUTH OUTL)
(TUPLE SET OUTL OUTH)
(STATE OUTL HIGH)
(STATE OUTH LOW)
****SKLRS****
(VOLTS OUTL 1.0799998)
*****************

<<<DESTROYING CB>>> TIME = 20.920000
STARTUP ** (S OUTL) (CVOLTS 0.19999999) (CRORIN 1) (CPTHRESH 2)

<<<CREATING CB>>> TIME = 20.920000
FINISHUP ** (S OUTL) (CVOLTS 2) (CRORIN 1) (CPTHRESH 2)

<<<DESTROYING CB>>> TIME = 22.320000
FINISHUP ** (S OUTL) (CVOLTS 2) (CRORIN 1) (CPTHRESH 2)

<<<DESTROYING CB>>> TIME = 30.180000
HIT ** (S SET) (CNBOUNCE 5)

<<<CREATING CB>>> TIME = 30.180000
STARTDN ** (S SET) (CVOLTS 3.4000000) (CRORIN 10) (CNTHRESH 0.7999999
9)

<<<DESTROYING CB>>> TIME = 30.440000
STARTDN ** (S SET) (CVOLTS 3.4000000) (CRORIN 10) (CNTHRESH 0.7999999
9)

<<<CREATING CB>>> TIME = 30.440000
FINISHDN ** (S SET) (CVOLTS 0.79999999) (CRORIN 10) (CNTHRESH 0.79999
999)

<<<CREATING CB>>> TIME = 30.440000
BOUNCE ** (S SET) (CNBOUNCE 5)

<<<DESTROYING CB>>> TIME = 30.5
FINISHDN ** (S SET) (CVOLTS 0.79999999) (CRORIN 10) (CNTHRESH 0.79999
999)
```

```
****TIME****
33
****EXPRS****
(UP RESET SET SW2)
(NBOUNCE SET 5)
(NBOUNCE RESET 0)
(CONTACT SET OFF)
(CONTACT RESET OFF)
(PHLIN SET 8)
(PHLIN RESET 8)
(PHLIN OUTH 0)
(PHLIN OUTL 0)
(PLHIN SET 12)
(PLHIN RESET 12)
(PLHIN OUTH 0)
(PLHIN OUTL 0)
(PULSEDN SET OFF)
(PULSEDN OUTH OFF)
(PULSEDN RESET OFF)
(PULSEDN OUTL OFF)
(PULSEUP OUTL OFF)
(PULSEUP SET OFF)
(PULSEUP RESET OFF)
(PULSEUP OUTH OFF)
(NTHRESH SET 0.79999999)
(NTHRESH RESET 0.79999999)
(NTHRESH OUTH 0.79999999)
(NTHRESH OUTL 0.79999999)
(PTHRESH SET 2.0)
(PTHRESH RESET 2.0)
(PTHRESH OUTH 2)
(PTHRESH OUTL 2)
(RORIN SET 10)
(RORIN RESET 10)
(RORIN OUTH 1)
(RORIN OUTL 1)
(VOLTS SET 0.20000056)
(VOLTS OUTL 3.4000000)
(VOLTS OUTH 0.19999997)
(VOLTS RESET 0.20000001)
(TYPE SET SIGNAL)
(TYPE RESET SIGNAL)
(TYPE OUTH SIGNAL)
(TYPE OUTL SIGNAL)
(TUPLE RESET OUTH OUTL)
(TUPLE SET OUTL OUTH)
(STATE OUTL HIGH)
(STATE OUTH LOW)
****SKLRS****
**********

<<<DESTROYING CB>>> TIME = 35.440000
BOUNCE ** (S SET) (CNBOUNCE 5)

<<<CREATING CB>>> TIME = 35.440000
STARTUP ** (S SET) (CVOLTS 0.20000056) (CRORIN 10) (CPTHRESH 2.0)

<<<DESTROYING CB>>> TIME = 35.619999
STARTUP ** (S SET) (CVOLTS 0.20000056) (CRORIN 10) (CPTHRESH 2.0)
```

```
<<<CREATING CB>>> TIME = 35.619999
FINISHUP ** (S SET) (CVOLTS 2.0) (CRORIN 10) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 35.619999
HIT ** (S SET) (CNBOUNCE NEW)

<<<DESTROYING CB>>> TIME = 35.759999
FINISHUP ** (S SET) (CVOLTS 2.0) (CRORIN 10) (CPTHRESH 2.0)

==========================
>>>BREAK AT 36
==========================

COMMAND: *PICTURE


****TIME****
36
****EXPRS****
(UP RESET SET SW2)
(NBOUNCE SET NEW)
(NBOUNCE RESET 0)
(CONTACT SET ON)
(CONTACT RESET OFF)
(PHLIN SET 8)
(PHLIN RESET 8)
(PHLIN OUTH 0)
(PHLIN OUTL 0)
(PLHIN SET 12)
(PLHIN RESET 12)
(PLHIN OUTH 0)
(PLHIN OUTL 0)
(PULSEDN SET OFF)
(PULSEDN OUTH OFF)
(PULSEDN RESET OFF)
(PULSEDN OUTL OFF)
(PULSEUP SET OFF)
(PULSEUP OUTL OFF)
(PULSEUP RESET OFF)
(PULSEUP OUTH OFF)
(NTHRESH SET 0.79999999)
(NTHRESH RESET 0.79999999)
(NTHRESH OUTH 0.79999999)
(NTHRESH OUTL 0.79999999)
(PTHRESH SET 2.0)
(PTHRESH RESET 2.0)
(PTHRESH OUTH 2)
(PTHRESH OUTL 2)
(RORIN SET 10)
(RORIN RESET 10)
(RORIN OUTH 1)
(RORIN OUTL 1)
(VOLTS SET 3.3999986)
(VOLTS OUTL 3.4000000)
(VOLTS OUTH 0.19999997)
(VOLTS RESET 0.20000001)
(TYPE SET SIGNAL)
(TYPE RESET SIGNAL)
(TYPE OUTH SIGNAL)
(TYPE OUTL SIGNAL)
```

```
(TUPLE RESET OUTH OUTL)
(TUPLE SET OUTL OUTH)
(STATE OUTL HIGH)
(STATE OUTH LOW)
****SKLRS****
******************

COMMAND: *(UNTRACE *)


COMMAND: *GO

==========================

COMMAND: *STOP

(****TERMINATED-AT-TIME 163.58000)
```

8. The One-Shot World

The one-shot (or monostable multivibrator) is a timing element which outputs a pulse of a specific duration when it is triggered. Available in integrated circuit packages, the chips are used in applications such as memory control which requires timing cycles different from a computer's synchronous clock. [7] This timing is achieved by means of resistors and capacitors used as inputs to the circuit. Typical output pulses for the 74121 one-shot range from 35 nanoseconds to 200 milliseconds. [6,p. 6-64]

The scenario CREATE-ONE-SHOT (Figure 8.1) contains all

```
(CREATE-ONE-SHOT(PAR A B D OH OL C CS R RS)
   (ICS(ALLOCATE-ACTIVATE CREATE-ONE-SHOT A B D OH OL C CS R RS))
   (EID(ALLOCATE-ACTIVATE CREATE-ONE-SHOT A B D OH OL C CS R RS))
   (EIA(ALLOCATE-ACTIVATE CREATE-SIGNAL A 0.2 1 1.4 1.4 45 50)
       (ALLOCATE-ACTIVATE CREATE-SIGNAL B 0.2 1 1.4 1.4 45 50)
       (ALLOCATE-ACTIVATE CREATE-SIGNAL D 0.2 0.1 1.35 1.55 35 40)
       (ALLOCATE-ACTIVATE CREATE-SIGNAL OH 0.2 1 1.4 1.4 0 0)
       (ALLOCATE-ACTIVATE CREATE-SIGNAL OL 3.4 1 1.4 1.4 0 0)
       (LEFTIN OH ZERO)(LEFTIN OL ZERO)
       (TUPLE A B D OH OL)(TUPLE B A D OH OL)
       (STATE OUT OFF)
       (TYPE C CAP)(STATE C CLOSED)(SIZE C CS)
       (TYPE R RES)(STATE R VCC)(RSIZE R RS)))
```

Figure 8.1

the relations necessary to form the SWM. There are three signal inputs and two output signals. All propagation delay values, the threshold values for the input signals, and the rate of rise of the inputs were taken from the specifications for the circuit. [6,p.6-65] The relation (STATE OUT OFF) is used to allow only one triggering input signal to have its effect on the output.

To obtain the scenarios needed to simulate a one-shot, the truth table for the circuit should be examined (Figure 8.2).

74121 ONE-SHOT Function Table				
INPUTS			OUTPUTS	
A1	A2	B	OUTH	OUTL
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⎍	⎍
↓	H	H	⎍	⎍
↓	↓	H	⎍	⎍
L	X	↑	⎍	⎍
X	L	↑	⎍	⎍

Figure 8.2

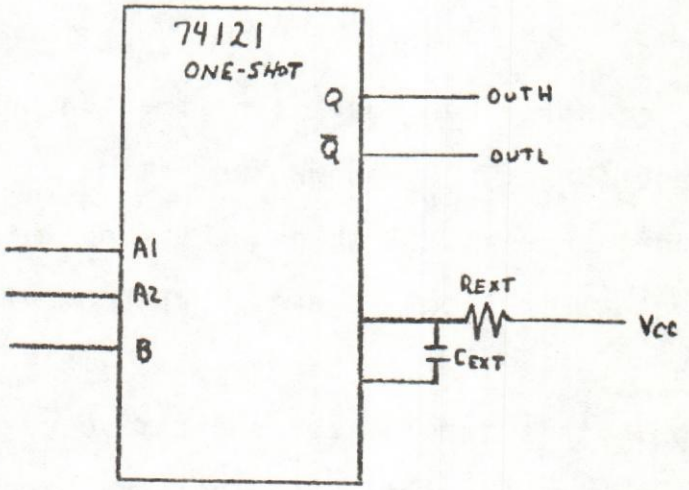


Figure 8.3

Only the lines of the truth table which result in an output pulse must be modeled. The three trigger scenarios accomplish this (Figure 8.4). By adding and extra TUPLE to the SWM,

```
(TRIGGERA(PAR Q R S O ONOT : CVOLTS PVOLTS)
   (ICS(TUPLE Q R S O ONOT)(STATE OUT OFF)
       (PULSEDN Q ON)(PULSEDN R OFF)(PULSEUP S OFF)
       (VOLTS R CVOLTS)(VOLTS S PVOLTS))
   (ICN(GT CVOLTS 1.4)(GT PVOLTS 1.4))
   (EID(STATE OUT OFF))
   (EIA(STATE OUT ON)(TRIGLH Q O)(TRIGHL Q ONOT)))

(TRIGGERAA(PAR Q R S O ONOT : CVOLTS)
   (ICS(TUPLE Q R S O ONOT)(STATE OUT OFF)
       (PULSEDN Q ON)(PULSEDN R ON)(PULSEUP S OFF)
       (VOLTS S CVOLTS))
   (ICN(GE CVOLTS 1.4))
   (EID(STATE OUT OFF))
   (EIA(STATE OUT ON)(TRIGLH Q O)(TRIGHL Q ONOT)))

(TRIGGERB(PAR Q R S O ONOT : CVOLTS)
   (ICS(TUPLE Q R S O ONOT)(STATE OUT OFF)
       (PULSE Q OFF)(PULSEUP S ON)(VOLTS Q CVOLTS))
   (ICN(LT CVOLTS 1.4))
   (EID(STATE OUT OFF))
   (EIA(STATE OUT ON)(TRIGLH S O)(TRIGHL S ONOT)))
```

Figure 8.4

one scenario can model two lines on the truth table. The trace (Example 6) shows the action of the one-shot. TRIGGERA uses the new TUPLE to cause the output pulse when either input A1 or input A2 has a PULSEDN relationship, and the other input is in a high state. TRIGGERAA handles the case when both A inputs are on negative edges, and TRIGGERB handles the positive edge cases. Since all inputs are ignored while there is an output pulse, the condition STATE OUT ON is added at this point. This prevents other activity on the inputs to affect the model until the output pulse is done.

Unlike a NOR gate or a flip-flop, the one-shot's output only remains high for a period of time determined by the

timing capacitors and resistors. Therefore, special OUTPUT-HIGH and OUTPUTLOW scenarios were developed (Figure 8.5). When the OUTH signal of the one-shot reaches its high level, OUTPUTHIGH is entered. Once entered, the scenario keeps the output at a high voltage level until either the CCS goes false (8.5.9), or until the interrupt time from the CCN is reached (8.5.10). The formula CSIZE * CRSIZE * 0.693147 is obtained as an approximation from the TI data book [6,6-64]. Other equations which more closely approximate the duration of the output pulse may easily be substituted in the CCN. When the interrupt time is reached, the signal is started down to the low level, and the STATE of OUT is set to OFF, allowing another input trigger to initiate an output pulse.

```
.1  (OUTPUTHIGH(PAR A B G Q D R C : CRORIN CVOLTS CRSIZE CSIZE)
.2     (ICS(TUPLE A B G Q D)(VOLTS Q CVOLTS)(RORIN Q CRORIN)
.3        (LEFTIN Q ZERO)(STATE OUT ON)
.4        (TYPE R RES)(RSIZE R CRSIZE)(STATE R VCC)
.5        (TYPE C CAP)(SIZE C CSIZE)(STATE C CLOSED))
.6     (ICN(GE CRSIZE 2)(LE CRSIZE 30)(EQUAL CVOLTS 3.4)
.7        (GE CSIZE 10)(LE CSIZE 10000000))
.8     (EID(LEFTIN Q *))
.9     (CCS(RSIZE R CRSIZE)(SIZE C CSIZE))
.10    (CCN FUNC (*PLUS % (*DIF(*TIMES CSIZE CRSIZE .693147)
.11                          (QUO 3.2 CRORIN))))
.12    (EPD(STATE OUT *))
.13    (EPA (STATE OUT OFF)(EDGE Q DN)(LEFTIN Q ZERO)))

.14 (OUTPUTLOW (PAR A B G D Q R C : CRORIN CVOLTS CRSIZE CSIZE)
.15     (ICS(TUPLE A B G D Q)(VOLTS Q CVOLTS)(RORIN Q CRORIN)
.16        (LEFTIN Q ZERO)(STATE OUT ON)(TYPE R RES)(RSIZE R CRSIZE)
.17        (STATE R VCC)(TYPE C CAP)(SIZE C CSIZE)(STATE C CLOSED))
.18     (ICN(GE CRSIZE 2)(LE CRSIZE 30)
.19        (EQUAL CVOLTS 0.2)
.20        (GE CSIZE 10)(LE CSIZE 10000000))
.21     (EID(LEFTIN Q *))
.22     (CCS(RSIZE R CRSIZE)(SIZE C CSIZE))
.23     (CCN FUNC (*PLUS % (*DIF(*TIMES CSIZE CRSIZE .693147)
.24                  (QUO 3.2 CRORIN))))
.25     (EPD(STATE OUT *))
.26     (EPA(STATE OUT OFF)(EDGE Q UP)(LEFTIN Q ZERO)))
```

Figure 8.5

Example 7 is a sample run of the one-shot world. After the SWM is created, a rising edge on input B is added. After the propagation delay, the output scenarios are initiated, and the output continues for 150.8 nanoseconds. Then, the outputs return to their normal states, waiting for additional input.

Example 7 -- The One-shot World

```
*(HSIM)

==========================
HENDRIX SIMULATION SYSTEM
==========================

INPUT SCENARIO LIST: *(EVAL SLIST)

STARTUP FINISHUP STARTDN FINISHDN TRIGGERA
TRIGGERAA TRIGGERB PROPDELAYLH PROPDELAYHL OUTPUTHIGH
OUTPUTLOW CREATE-SIGNAL CREATE-ONE-SHOT

INPUT SWM RELATION LIST: *(EVAL SWM)


COMMAND: *(TRACE *)


COMMAND: *(SNAPSHOTS 16 55 75)


COMMAND: *(ADD(ALLOCATE-ACTIVATE CREATE-ONE-SHOT A1 A2 B OUTH OUTL
*CEXT 30 REXT 5))


COMMAND: *GO


<<<CREATING CB>>> TIME = 0
CREATE-ONE-SHOT ** (A A1) (B A2) (D B) (OH OUTH) (OL OUTL) (C CEXT) (
CS 30) (R REXT) (RS 5)

<<<DESTROYING CB>>> TIME = 0
CREATE-ONE-SHOT ** (A A1) (B A2) (D B) (OH OUTH) (OL OUTL) (C CEXT) (
CS 30) (R REXT) (RS 5)

<<<CREATING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG OUTL) (CVOLTS 3.4000000) (CRATE 1) (PT 1.400000
0) (NT 1.4000000) (PLH 0) (PHL 0)

<<<DESTROYING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG OUTL) (CVOLTS 3.4000000) (CRATE 1) (PT 1.400000
0) (NT 1.4000000) (PLH 0) (PHL 0)

<<<CREATING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG OUTH) (CVOLTS 0.19999999) (CRATE 1) (PT 1.40000
00) (NT 1.4000000) (PLH 0) (PHL 0)

<<<DESTROYING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG OUTH) (CVOLTS 0.19999999) (CRATE 1) (PT 1.40000
00) (NT 1.4000000) (PLH 0) (PHL 0)

<<<CREATING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG B) (CVOLTS 0.19999999) (CRATE 0.09999999) (PT 1
.5499999) (NT 1.3500000) (PLH 35) (PHL 40)
```

```
<<<DESTROYING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG B) (CVOLTS 0.19999999) (CRATE 0.09999999) (PT 1
.5499999) (NT 1.3500000) (PLH 35) (PHL 40)

<<<CREATING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG A2) (CVOLTS 0.19999999) (CRATE 1) (PT 1.4000000
) (NT 1.4000000) (PLH 45) (PHL 50)

<<<DESTROYING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG A2) (CVOLTS 0.19999999) (CRATE 1) (PT 1.4000000
) (NT 1.4000000) (PLH 45) (PHL 50)

<<<CREATING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG A1) (CVOLTS 0.19999999) (CRATE 1) (PT 1.4000000
) (NT 1.4000000) (PLH 45) (PHL 50)

<<<DESTROYING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG A1) (CVOLTS 0.19999999) (CRATE 1) (PT 1.4000000
) (NT 1.4000000) (PLH 45) (PHL 50)

COMMAND: *(ADD(EDGE B UP))


COMMAND: *GO


<<<CREATING CB>>> TIME = 0
STARTUP ** (S B) (CVOLTS 0.19999999) (CRORIN 0.09999999) (CPTHRESH 1.
5499999)

<<<DESTROYING CB>>> TIME = 13.5
STARTUP ** (S B) (CVOLTS 0.19999999) (CRORIN 0.09999999) (CPTHRESH 1.
5499999)

<<<CREATING CB>>> TIME = 13.5
FINISHUP ** (S B) (CVOLTS 1.5499999) (CRORIN 0.09999999) (CPTHRESH 1.
5499999)

<<<CREATING CB>>> TIME = 13.5
TRIGGERB ** (Q A2) (R A1) (S B) (O OUTH) (ONOT OUTL) (CVOLTS 0.199999
99)

<<<DESTROYING CB>>> TIME = 13.5
TRIGGERB ** (Q A2) (R A1) (S B) (O OUTH) (ONOT OUTL) (CVOLTS 0.199999
99)

<<<CREATING CB>>> TIME = 13.5
PROPDELAYLH ** (Q B) (L OUTH) (CPLHIN 35) (CRORIN 1) (CVOLTS 0.199999
99) (CPTHRESH 1.4000000)

<<<CREATING CB>>> TIME = 13.5
PROPDELAYHL ** (Q B) (Z OUTL) (CPHLIN 40) (CRORIN 1) (CVOLTS 3.400000
0) (CNTHRESH 1.4000000)

****TIME****
16
****EXPRS****
(PHLIN A1 50)
(PHLIN A2 50)
```

```
(PHLIN B 40)
(PHLIN OUTH 0)
(PHLIN OUTL 0)
(PLHIN A1 45)
(PLHIN A2 45)
(PLHIN B 35)
(PLHIN OUTH 0)
(PLHIN OUTL 0)
(PULSEDN A1 OFF)
(PULSEDN A2 OFF)
(PULSEDN B OFF)
(PULSEDN OUTH OFF)
(PULSEDN OUTL OFF)
(PULSEUP B ON)
(PULSEUP A1 OFF)
(PULSEUP A2 OFF)
(PULSEUP OUTH OFF)
(PULSEUP OUTL OFF)
(NTHRESH A1 1.4000000)
(NTHRESH A2 1.4000000)
(NTHRESH B 1.3500000)
(NTHRESH OUTH 1.4000000)
(NTHRESH OUTL 1.4000000)
(PTHRESH A1 1.4000000)
(PTHRESH A2 1.4000000)
(PTHRESH B 1.5499999)
(PTHRESH OUTH 1.4000000)
(PTHRESH OUTL 1.4000000)
(RORIN A1 1)
(RORIN A2 1)
(RORIN B 0.09999999)
(RORIN OUTH 1)
(RORIN OUTL 1)
(VOLTS A1 0.19999999)
(VOLTS A2 0.19999999)
(VOLTS OUTH 0.19999999)
(VOLTS OUTL 3.4000000)
(RSIZE REXT 5)
(SIZE CEXT 30)
(TYPE A1 SIGNAL)
(TYPE A2 SIGNAL)
(TYPE B SIGNAL)
(TYPE OUTH SIGNAL)
(TYPE OUTL SIGNAL)
(TYPE REXT RES)
(TYPE CEXT CAP)
(STATE OUT ON)
(STATE REXT VCC)
(STATE CEXT CLOSED)
(TUPLE A2 A1 B OUTH OUTL)
(TUPLE A1 A2 B OUTH OUTL)
(LEFTIN OUTL ZERO)
(LEFTIN OUTH ZERO)
****SKLRS****
(VOLTS B 1.7999999)
*****************

<<<DESTROYING CB>>> TIME = 32.000000
FINISHUP ** (S B) (CVOLTS 1.5499999) (CRORIN 0.09999999) (CPTHRESH 1.
5499999)
```

```
<<<DESTROYING CB>>> TIME = 47.300000
PROPDELAYLH ** (Q B) (L OUTH) (CPLHIN 35) (CRORIN 1) (CVOLTS 0.199999
99) (CPTHRESH 1.4000000)

<<<CREATING CB>>> TIME = 47.300000
STARTUP ** (S OUTH) (CVOLTS 0.19999999) (CRORIN 1) (CPTHRESH 1.400000
0)

<<<DESTROYING CB>>> TIME = 48.5
STARTUP ** (S OUTH) (CVOLTS 0.19999999) (CRORIN 1) (CPTHRESH 1.400000
0)

<<<CREATING CB>>> TIME = 48.5
FINISHUP ** (S OUTH) (CVOLTS 1.4000000) (CRORIN 1) (CPTHRESH 1.400000
0)

<<<DESTROYING CB>>> TIME = 50.5
FINISHUP ** (S OUTH) (CVOLTS 1.4000000) (CRORIN 1) (CPTHRESH 1.400000
0)

<<<CREATING CB>>> TIME = 50.5
OUTPUTHIGH ** (A A2) (B A1) (G B) (Q OUTH) (D OUTL) (R REXT) (C CEXT)
 (CRORIN 1) (CVOLTS 3.4000000) (CRSIZE 5) (CSIZE 30)

<<<DESTROYING CB>>> TIME = 51.5
PROPDELAYHL ** (Q B) (Z OUTL) (CPHLIN 40) (CRORIN 1) (CVOLTS 3.400000
0) (CNTHRESH 1.4000000)

<<<CREATING CB>>> TIME = 51.5
STARTDN ** (S OUTL) (CVOLTS 3.4000000) (CRORIN 1) (CNTHRESH 1.4000000
)

<<<DESTROYING CB>>> TIME = 53.5
STARTDN ** (S OUTL) (CVOLTS 3.4000000) (CRORIN 1) (CNTHRESH 1.4000000
)

<<<CREATING CB>>> TIME = 53.5
FINISHDN ** (S OUTL) (CVOLTS 1.4000000) (CRORIN 1) (CNTHRESH 1.400000
0)

<<<DESTROYING CB>>> TIME = 54.699999
FINISHDN ** (S OUTL) (CVOLTS 1.4000000) (CRORIN 1) (CNTHRESH 1.400000
0)

<<<CREATING CB>>> TIME = 54.699999
OUTPUTLOW ** (A A2) (B A1) (G B) (D OUTH) (Q OUTL) (R REXT) (C CEXT)
(CRORIN 1) (CVOLTS 0.20000019) (CRSIZE 5) (CSIZE 30)

****TIME****
75
****EXPRS****
(PHLIN A1 50)
(PHLIN A2 50)
(PHLIN B 40)
(PHLIN OUTH 0)
(PHLIN OUTL 0)
(PLHIN A1 45)
(PLHIN A2 45)
(PLHIN B 35)
(PLHIN OUTH 0)
```

```
(PLHIN OUTL 0)
(PULSEDN OUTL OFF)
(PULSEDN A1 OFF)
(PULSEDN A2 OFF)
(PULSEDN B OFF)
(PULSEDN OUTH OFF)
(PULSEUP OUTH OFF)
(PULSEUP B OFF)
(PULSEUP A1 OFF)
(PULSEUP A2 OFF)
(PULSEUP OUTL OFF)
(NTHRESH A1 1.4000000)
(NTHRESH A2 1.4000000)
(NTHRESH B 1.3500000)
(NTHRESH OUTH 1.4000000)
(NTHRESH OUTL 1.4000000)
(PTHRESH A1 1.4000000)
(PTHRESH A2 1.4000000)
(PTHRESH B 1.5499999)
(PTHRESH OUTH 1.4000000)
(PTHRESH OUTL 1.4000000)
(RORIN A1 1)
(RORIN A2 1)
(RORIN B 0.09999999)
(RORIN OUTH 1)
(RORIN OUTL 1)
(VOLTS OUTL 0.20000019)
(VOLTS OUTH 3.4000000)
(VOLTS B 3.4000000)
(VOLTS A1 0.19999999)
(VOLTS A2 0.19999999)
(RSIZE REXT 5)
(SIZE CEXT 30)
(TYPE A1 SIGNAL)
(TYPE A2 SIGNAL)
(TYPE B SIGNAL)
(TYPE OUTH SIGNAL)
(TYPE OUTL SIGNAL)
(TYPE REXT RES)
(TYPE CEXT CAP)
(STATE OUT ON)
(STATE REXT VCC)
(STATE CEXT CLOSED)
(TUPLE A2 A1 B OUTH OUTL)
(TUPLE A1 A2 B OUTH OUTL)
****SKLRS****
*****************

<<<DESTROYING CB>>> TIME = 197.29999
OUTPUTHIGH ** (A A2) (B A1) (G B) (Q OUTH) (D OUTL) (R REXT) (C CEXT)
 (CRORIN 1) (CVOLTS 3.4000000) (CRSIZE 5) (CSIZE 30)

<<<CREATING CB>>> TIME = 197.29999
STARTDN ** (S OUTH) (CVOLTS 3.4000000) (CRORIN 1) (CNTHRESH 1.4000000
)

<<<DESTROYING CB>>> TIME = 199.29999
STARTDN ** (S OUTH) (CVOLTS 3.4000000) (CRORIN 1) (CNTHRESH 1.4000000
)
```

```
<<<CREATING CB>>> TIME = 199.29999
FINISHDN ** (S OUTH) (CVOLTS 1.4000000) (CRORIN 1) (CNTHRESH 1.400000
0)

<<<DESTROYING CB>>> TIME = 200.5
FINISHDN ** (S OUTH) (CVOLTS 1.4000000) (CRORIN 1) (CNTHRESH 1.400000
0)

<<<DESTROYING CB>>> TIME = 201.5
OUTPUTLOW ** (A A2) (B A1) (G B) (D OUTH) (Q OUTL) (R REXT) (C CEXT)
(CRORIN 1) (CVOLTS 0.20000019) (CRSIZE 5) (CSIZE 30)

<<<CREATING CB>>> TIME = 201.5
STARTUP ** (S OUTL) (CVOLTS 0.20000019) (CRORIN 1) (CPTHRESH 1.400000
0)

<<<DESTROYING CB>>> TIME = 202.70000
STARTUP ** (S OUTL) (CVOLTS 0.20000019) (CRORIN 1) (CPTHRESH 1.400000
0)

<<<CREATING CB>>> TIME = 202.70000
FINISHUP ** (S OUTL) (CVOLTS 1.4000000) (CRORIN 1) (CPTHRESH 1.400000
0)

<<<DESTROYING CB>>> TIME = 204.70000
FINISHUP ** (S OUTL) (CVOLTS 1.4000000) (CRORIN 1) (CPTHRESH 1.400000
0)

COMMAND: *PICTURE


****TIME****
204.70000
****EXPRS****
(PHLIN A1 50)
(PHLIN A2 50)
(PHLIN B 40)
(PHLIN OUTH 0)
(PHLIN OUTL 0)
(PLHIN A1 45)
(PLHIN A2 45)
(PLHIN B 35)
(PLHIN OUTH 0)
(PLHIN OUTL 0)
(PULSEDN OUTH OFF)
(PULSEDN OUTL OFF)
(PULSEDN A1 OFF)
(PULSEDN A2 OFF)
(PULSEDN B OFF)
(PULSEUP OUTL OFF)
(PULSEUP OUTH OFF)
(PULSEUP B OFF)
(PULSEUP A1 OFF)
(PULSEUP A2 OFF)
(NTHRESH A1 1.4000000)
(NTHRESH A2 1.4000000)
(NTHRESH B 1.3500000)
(NTHRESH OUTH 1.4000000)
(NTHRESH OUTL 1.4000000)
(PTHRESH A1 1.4000000)
```

```
(PTHRESH A2 1.4000000)
(PTHRESH B 1.5499999)
(PTHRESH OUTH 1.4000000)
(PTHRESH OUTL 1.4000000)
(RORIN A1 1)
(RORIN A2 1)
(RORIN B 0.09999999)
(RORIN OUTH 1)
(RORIN OUTL 1)
(VOLTS OUTL 3.4000000)
(VOLTS OUTH 0.19999924)
(VOLTS B 3.4000000)
(VOLTS A1 0.19999999)
(VOLTS A2 0.19999999)
(RSIZE REXT 5)
(SIZE CEXT 30)
(TYPE A1 SIGNAL)
(TYPE A2 SIGNAL)
(TYPE B SIGNAL)
(TYPE OUTH SIGNAL)
(TYPE OUTL SIGNAL)
(TYPE REXT RES)
(TYPE CEXT CAP)
(STATE OUT OFF)
(STATE REXT VCC)
(STATE CEXT CLOSED)
(TUPLE A2 A1 B OUTH OUTL)
(TUPLE A1 A2 B OUTH OUTL)
(LEFTIN OUTL ZERO)
(LEFTIN OUTH ZERO)
****SKLRS****
*****************

COMMAND: *STOP

(****TERMINATED-AT-TIME**** 204.70000)
```

9. Debounced Inputs to the One-shot

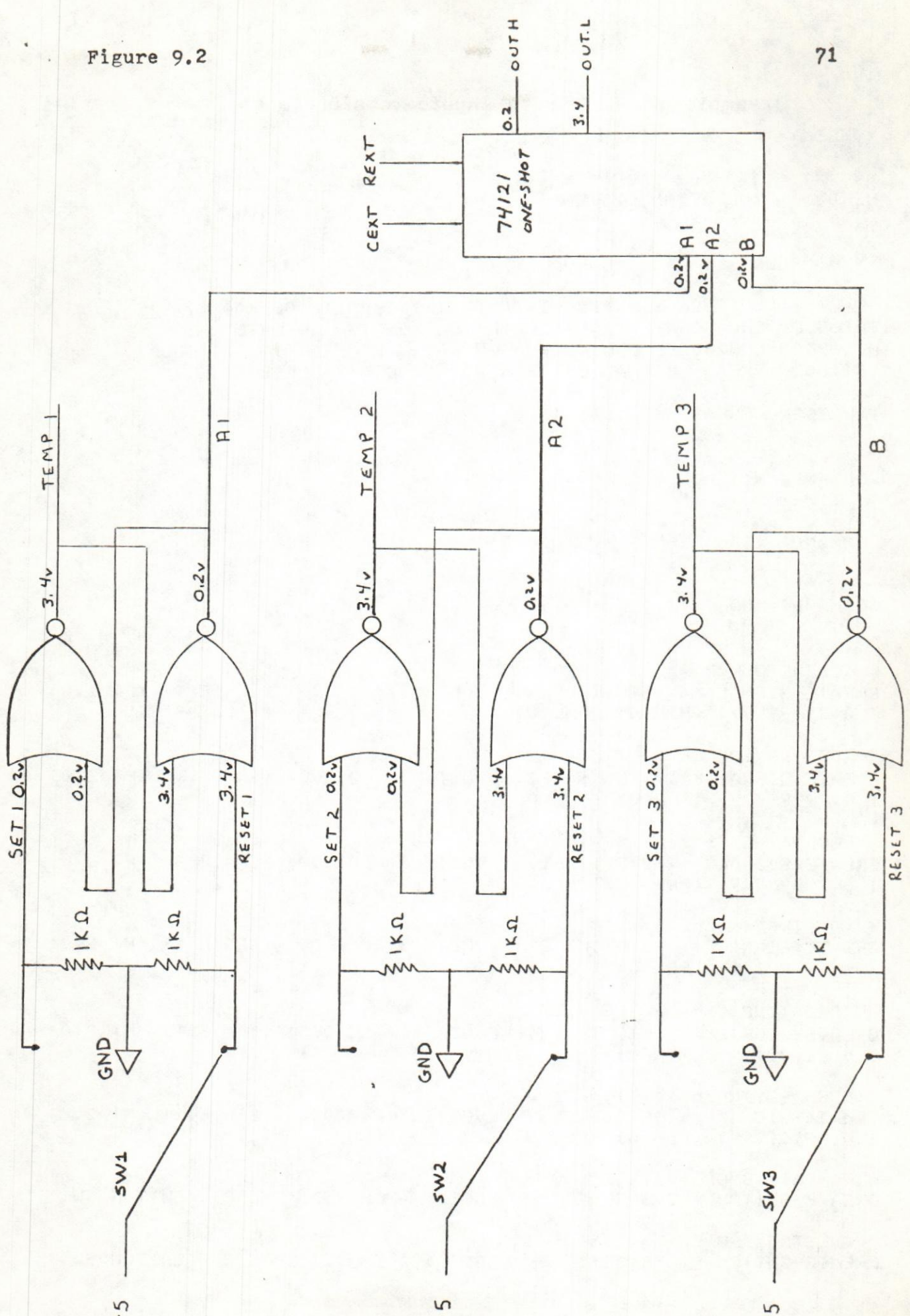
An interesting exercise of the model is to use debounced switches as described in section 7 as inputs to the one-shot just completed. This requires fourteen signals to be modeled. The SWM to create these signals is shown in Figure 9.1. The three switches are created (9.1.1-9.1.3) and a one-shot is then created (9.1.4). Then, the extra TEMPorary signals needed to debounce the switches, and the TUPLES are added to the SWM. Such a configuration with initial voltage levels is shown in Figure 9.2.

```
.1 (ALLOCATE-ACTIVATE CREATE-SWITCH SET1 RESET1 12 8 SW1)
.2 (ALLOCATE-ACTIVATE CREATE-SWITCH SET2 RESET2 12 8 SW2)
.3 (ALLOCATE-ACTIVATE CREATE-SWITCH SET3 RESET3 12 8 SW3)
.4 (ALLOCATE-ACTIVATE CREATE-ONE-SHOT A1 A2 B OUTH OUTL CEXT 30
.5                RINT 2)
.6 (ALLOCATE-ACTIVATE CREATE-SIGNAL TEMP1 3.4 1 2.0 0.8 0 0)
.7 (ALLOCATE-ACTIVATE CREATE-SIGNAL TEMP2 3.4 1 2.0 0.8 0 0)
.8 (ALLOCATE-ACTIVATE CREATE-SIGNAL TEMP3 3.4 1 2.0 0.8 0 0)
.9 (TUPLE RESET1 TEMP1 A1)
.10(TUPLE SET1 A1 TEMP1)
.11(TUPLE RESET2 TEMP2 A2)
.12(TUPLE SET2 A2 TEMP2)
.13(TUPLE RESET3 TEMP3 B)
.14(TUPLE SET3 B TEMP3)
.15(STATE A1 LOW)(STATE A2 LOW)(STATE B LOW)
.16(STATE TEMP1 HIGH)(STATE TEMP2 HIGH)(STATE TEMP3 HIGH)
```

Figure 9.1

Example 8 is a sample of the output produced by the circuit described above. SW3 is thrown upward, causing the B input to have a positive edge, which triggers the one-shot. Notice that the switch is still bouncing even after the output pulses have been completed.

Figure 9.2


74121
ONE-SHOT
CEXT REXT
OUT H
OUT L
0.2
3.4
A1
A2
B
TEMP 1
TEMP 2
TEMP 3
SET 1 0.2v
SET 2 0.2v
SET 3 0.2v
RESET 1
RESET 2
RESET 3
1KΩ
GND
SW1
SW2
SW3
+5

Example 8---Debounced Inputs to a One-shot

```
*(HSIM)

==========================
HENDRIX SIMULATION SYSTEM
==========================

INPUT SCENARIO LIST: *(EVAL SLIST)

STARTUP FINISHUP STARTDN FINISHDN TRIGGERA TRIGGERAA
TRIGGERB PROPDELAYLH PROPDELAYHL OUTPUTHIGH OUTPUTLOW
HIGH7402 LOW7402-1 LOW7402-2 LOW7402-3 BOUNCE HIT SWITCHUP
SWITCHDN CREATE-SIGNAL CREATE-SWITCH CREATE-ONE-SHOT

INPUT SWM RELATION LIST: *(EVAL SWM)


COMMAND: *(TRACE *)


COMMAND: *(SNAPSHOTS 19 90)


COMMAND: *GO


<<<CREATING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG TEMP1) (CVOLTS 3.4000000) (CRATE 1) (PT 2.0) (N
T 0.79999999) (PLH 0) (PHL 0)

<<<DESTROYING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG TEMP1) (CVOLTS 3.4000000) (CRATE 1) (PT 2.0) (N
T 0.79999999) (PLH 0) (PHL 0)

<<<CREATING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG TEMP2) (CVOLTS 3.4000000) (CRATE 1) (PT 2.0) (N
T 0.79999999) (PLH 0) (PHL 0)

<<<DESTROYING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG TEMP2) (CVOLTS 3.4000000) (CRATE 1) (PT 2.0) (N
T 0.79999999) (PLH 0) (PHL 0)

<<<CREATING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG TEMP3) (CVOLTS 3.4000000) (CRATE 1) (PT 2.0) (N
T 0.79999999) (PLH 0) (PHL 0)

<<<DESTROYING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG TEMP3) (CVOLTS 3.4000000) (CRATE 1) (PT 2.0) (N
T 0.79999999) (PLH 0) (PHL 0)

<<<CREATING CB>>> TIME = 0
CREATE-SWITCH ** (S SET1) (R RESET1) (PLH 12) (PHL 8) (SWITCH SW1)

<<<DESTROYING CB>>> TIME = 0
CREATE-SWITCH ** (S SET1) (R RESET1) (PLH 12) (PHL 8) (SWITCH SW1)
```

```
<<<CREATING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG RESET1) (CVOLTS 3.4000000) (CRATE 10) (PT 2.0)
(NT 0.79999999) (PLH 12) (PHL 8)

<<<DESTROYING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG RESET1) (CVOLTS 3.4000000) (CRATE 10) (PT 2.0)
(NT 0.79999999) (PLH 12) (PHL 8)

<<<CREATING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG SET1) (CVOLTS 0.19999999) (CRATE 10) (PT 2.0) (
NT 0.79999999) (PLH 12) (PHL 8)

<<<DESTROYING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG SET1) (CVOLTS 0.19999999) (CRATE 10) (PT 2.0) (
NT 0.79999999) (PLH 12) (PHL 8)

<<<CREATING CB>>> TIME = 0
CREATE-SWITCH ** (S SET2) (R RESET2) (PLH 12) (PHL 8) (SWITCH SW2)

<<<DESTROYING CB>>> TIME = 0
CREATE-SWITCH ** (S SET2) (R RESET2) (PLH 12) (PHL 8) (SWITCH SW2)

<<<CREATING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG RESET2) (CVOLTS 3.4000000) (CRATE 10) (PT 2.0)
(NT 0.79999999) (PLH 12) (PHL 8)

<<<DESTROYING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG RESET2) (CVOLTS 3.4000000) (CRATE 10) (PT 2.0)
(NT 0.79999999) (PLH 12) (PHL 8)

<<<CREATING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG SET2) (CVOLTS 0.19999999) (CRATE 10) (PT 2.0) (
NT 0.79999999) (PLH 12) (PHL 8)

<<<DESTROYING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG SET2) (CVOLTS 0.19999999) (CRATE 10) (PT 2.0) (
NT 0.79999999) (PLH 12) (PHL 8)

<<<CREATING CB>>> TIME = 0
CREATE-SWITCH ** (S SET3) (R RESET3) (PLH 12) (PHL 8) (SWITCH SW3)

<<<DESTROYING CB>>> TIME = 0
CREATE-SWITCH ** (S SET3) (R RESET3) (PLH 12) (PHL 8) (SWITCH SW3)

<<<CREATING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG RESET3) (CVOLTS 3.4000000) (CRATE 10) (PT 2.0)
(NT 0.79999999) (PLH 12) (PHL 8)

<<<DESTROYING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG RESET3) (CVOLTS 3.4000000) (CRATE 10) (PT 2.0)
(NT 0.79999999) (PLH 12) (PHL 8)

<<<CREATING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG SET3) (CVOLTS 0.19999999) (CRATE 10) (PT 2.0) (
NT 0.79999999) (PLH 12) (PHL 8)

<<<DESTROYING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG SET3) (CVOLTS 0.19999999) (CRATE 10) (PT 2.0) (
NT 0.79999999) (PLH 12) (PHL 8)
```

```
<<<CREATING CB>>> TIME = 0
CREATE-ONE-SHOT ** (A A1) (B A2) (D B) (OH OUTH) (OL OUTL) (C CEXT) (
CS 30) (R RINT) (RS 2)

<<<DESTROYING CB>>> TIME = 0
CREATE-ONE-SHOT ** (A A1) (B A2) (D B) (OH OUTH) (OL OUTL) (C CEXT) (
CS 30) (R RINT) (RS 2)

<<<CREATING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG OUTL) (CVOLTS 3.4000000) (CRATE 1) (PT 1.400000
0) (NT 1.4000000) (PLH 0) (PHL 0)

<<<DESTROYING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG OUTL) (CVOLTS 3.4000000) (CRATE 1) (PT 1.400000
0) (NT 1.4000000) (PLH 0) (PHL 0)

<<<CREATING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG OUTH) (CVOLTS 0.19999999) (CRATE 1) (PT 1.40000
00) (NT 1.4000000) (PLH 0) (PHL 0)

<<<DESTROYING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG OUTH) (CVOLTS 0.19999999) (CRATE 1) (PT 1.40000
00) (NT 1.4000000) (PLH 0) (PHL 0)

<<<CREATING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG B) (CVOLTS 0.19999999) (CRATE 0.09999999) (PT 1
.5499999) (NT 1.3500000) (PLH 35) (PHL 40)

<<<DESTROYING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG B) (CVOLTS 0.19999999) (CRATE 0.09999999) (PT 1
.5499999) (NT 1.3500000) (PLH 35) (PHL 40)

<<<CREATING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG A2) (CVOLTS 0.19999999) (CRATE 1) (PT 1.4000000
) (NT 1.4000000) (PLH 45) (PHL 50)

<<<DESTROYING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG A2) (CVOLTS 0.19999999) (CRATE 1) (PT 1.4000000
) (NT 1.4000000) (PLH 45) (PHL 50)

<<<CREATING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG A1) (CVOLTS 0.19999999) (CRATE 1) (PT 1.4000000
) (NT 1.4000000) (PLH 45) (PHL 50)

<<<DESTROYING CB>>> TIME = 0
CREATE-SIGNAL ** (SIG A1) (CVOLTS 0.19999999) (CRATE 1) (PT 1.4000000
) (NT 1.4000000) (PLH 45) (PHL 50)

COMMAND: *(ADD(ALLOCATE-ACTIVATE SWITCHUP SW3))


COMMAND: *GO


<<<CREATING CB>>> TIME = 0
SWITCHUP ** (R RESET3) (S SET3) (T SW3)

<<<DESTROYING CB>>> TIME = 0
SWITCHUP ** (R RESET3) (S SET3) (T SW3)
```

```
<<<CREATING CB>>> TIME = 0
STARTUP ** (S SET3) (CVOLTS 0.19999999) (CRORIN 10) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 0
STARTDN ** (S RESET3) (CVOLTS 3.4000000) (CRORIN 10) (CNTHRESH 0.7999
9999)

<<<DESTROYING CB>>> TIME = 0.17999999
STARTUP ** (S SET3) (CVOLTS 0.19999999) (CRORIN 10) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 0.17999999
FINISHUP ** (S SET3) (CVOLTS 2.0) (CRORIN 10) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 0.17999999
HIT ** (S SET3) (CNBOUNCE 5)

<<<DESTROYING CB>>> TIME = 0.26000000
STARTDN ** (S RESET3) (CVOLTS 3.4000000) (CRORIN 10) (CNTHRESH 0.7999
9999)

<<<CREATING CB>>> TIME = 0.26000000
FINISHDN ** (S RESET3) (CVOLTS 0.79999999) (CRORIN 10) (CNTHRESH 0.79
999999)

<<<DESTROYING CB>>> TIME = 0.32000000
FINISHDN ** (S RESET3) (CVOLTS 0.79999999) (CRORIN 10) (CNTHRESH 0.79
999999)

<<<DESTROYING CB>>> TIME = 0.32000000
FINISHUP ** (S SET3) (CVOLTS 2.0) (CRORIN 10) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 0.32000000
LOW7402-2 ** (IN1 SET3) (IN2 B) (OUT1 TEMP3) (CVIN1 3.4000000) (CVIN2
 0.19999999) (CVOUT 3.4000000) (CNTHRESH 1.3500000) (CPTHRESH 2.0)

<<<DESTROYING CB>>> TIME = 0.32000000
LOW7402-2 ** (IN1 SET3) (IN2 B) (OUT1 TEMP3) (CVIN1 3.4000000) (CVIN2
 0.19999999) (CVOUT 3.4000000) (CNTHRESH 1.3500000) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 0.32000000
PROPDELAYHL ** (Q SET3) (Z TEMP3) (CPHLIN 8) (CRORIN 1) (CVOLTS 3.400
0000) (CNTHRESH 0.79999999)

<<<DESTROYING CB>>> TIME = 5.7199999
PROPDELAYHL ** (Q SET3) (Z TEMP3) (CPHLIN 8) (CRORIN 1) (CVOLTS 3.400
0000) (CNTHRESH 0.79999999)

<<<CREATING CB>>> TIME = 5.7199999
STARTDN ** (S TEMP3) (CVOLTS 3.4000000) (CRORIN 1) (CNTHRESH 0.799999
99)

<<<DESTROYING CB>>> TIME = 8.3200000
STARTDN ** (S TEMP3) (CVOLTS 3.4000000) (CRORIN 1) (CNTHRESH 0.799999
99)

<<<CREATING CB>>> TIME = 8.3200000
FINISHDN ** (S TEMP3) (CVOLTS 0.79999999) (CRORIN 1) (CNTHRESH 0.7999
9999)
```

```
<<<DESTROYING CB>>> TIME = 8.9200000
FINISHDN ** (S TEMP3) (CVOLTS 0.79999999) (CRORIN 1) (CNTHRESH 0.7999
9999)

<<<CREATING CB>>> TIME = 8.9200000
HIGH7402 ** (IN1 RESET3) (IN2 TEMP3) (OUT1 B) (CVIN1 0.20000001) (CVI
N2 0.19999997) (CVOUT 0.19999999) (CPTHRESH 1.5499999) (CNTHRESH 0.79
999999)

<<<DESTROYING CB>>> TIME = 8.9200000
HIGH7402 ** (IN1 RESET3) (IN2 TEMP3) (OUT1 B) (CVIN1 0.20000001) (CVI
N2 0.19999997) (CVOUT 0.19999999) (CPTHRESH 1.5499999) (CNTHRESH 0.79
999999)

<<<CREATING CB>>> TIME = 8.9200000
PROPDELAYLH ** (Q RESET3) (L B) (CPLHIN 12) (CRORIN 0.09999999) (CVOL
TS 0.19999999) (CPTHRESH 1.5499999)

<<<DESTROYING CB>>> TIME = 7.4200000
PROPDELAYLH ** (Q RESET3) (L B) (CPLHIN 12) (CRORIN 0.09999999) (CVOL
TS 0.19999999) (CPTHRESH 1.5499999)

<<<CREATING CB>>> TIME = 7.4200000
STARTUP ** (S B) (CVOLTS 0.19999999) (CRORIN 0.09999999) (CPTHRESH 1.
5499999)

****TIME****
19
****EXPRS****
(UP RESET3 SET3 SW3)
(RSIZE RINT 2)
(SIZE CEXT 30)
(LEFTIN OUTL ZERO)
(LEFTIN OUTH ZERO)
(NBOUNCE SET3 5)
(NBOUNCE RESET3 0)
(NBOUNCE SET2 0)
(NBOUNCE RESET2 0)
(NBOUNCE SET1 0)
(NBOUNCE RESET1 0)
(CONTACT SET3 ON)
(CONTACT RESET3 OFF)
(CONTACT SET2 OFF)
(CONTACT RESET2 ON)
(CONTACT SET1 OFF)
(CONTACT RESET1 ON)
(DOWN RESET2 SET2 SW2)
(DOWN RESET1 SET1 SW1)
(PHLIN A1 50)
(PHLIN A2 50)
(PHLIN B 40)
(PHLIN OUTH 0)
(PHLIN OUTL 0)
(PHLIN SET3 8)
(PHLIN RESET3 8)
(PHLIN SET2 8)
(PHLIN RESET2 8)
(PHLIN SET1 8)
(PHLIN RESET1 8)
(PHLIN TEMP3 0)
```

```
(PHLIN TEMP2 0)
(PHLIN TEMP1 0)
(PLHIN A1 45)
(PLHIN A2 45)
(PLHIN B 35)
(PLHIN OUTH 0)
(PLHIN OUTL 0)
(PLHIN SET3 12)
(PLHIN RESET3 12)
(PLHIN SET2 12)
(PLHIN RESET2 12)
(PLHIN SET1 12)
(PLHIN RESET1 12)
(PLHIN TEMP3 0)
(PLHIN TEMP2 0)
(PLHIN TEMP1 0)
(PULSEDN TEMP3 OFF)
(PULSEDN RESET3 OFF)
(PULSEDN A1 OFF)
(PULSEDN A2 OFF)
(PULSEDN B OFF)
(PULSEDN OUTH OFF)
(PULSEDN OUTL OFF)
(PULSEDN SET3 OFF)
(PULSEDN SET2 OFF)
(PULSEDN RESET2 OFF)
(PULSEDN SET1 OFF)
(PULSEDN RESET1 OFF)
(PULSEDN TEMP2 OFF)
(PULSEDN TEMP1 OFF)
(PULSEUP SET3 OFF)
(PULSEUP A1 OFF)
(PULSEUP A2 OFF)
(PULSEUP B OFF)
(PULSEUP OUTH OFF)
(PULSEUP OUTL OFF)
(PULSEUP RESET3 OFF)
(PULSEUP SET2 OFF)
(PULSEUP RESET2 OFF)
(PULSEUP SET1 OFF)
(PULSEUP RESET1 OFF)
(PULSEUP TEMP3 OFF)
(PULSEUP TEMP2 OFF)
(PULSEUP TEMP1 OFF)
(NTHRESH A1 1.4000000)
(NTHRESH A2 1.4000000)
(NTHRESH B 1.3500000)
(NTHRESH OUTH 1.4000000)
(NTHRESH OUTL 1.4000000)
(NTHRESH SET3 0.79999999)
(NTHRESH RESET3 0.79999999)
(NTHRESH SET2 0.79999999)
(NTHRESH RESET2 0.79999999)
(NTHRESH SET1 0.79999999)
(NTHRESH RESET1 0.79999999)
(NTHRESH TEMP3 0.79999999)
(NTHRESH TEMP2 0.79999999)
(NTHRESH TEMP1 0.79999999)
(PTHRESH A1 1.4000000)
(PTHRESH A2 1.4000000)
```

```
(PTHRESH B 1.5499999)
(PTHRESH OUTH 1.4000000)
(PTHRESH OUTL 1.4000000)
(PTHRESH SET3 2.0)
(PTHRESH RESET3 2.0)
(PTHRESH SET2 2.0)
(PTHRESH RESET2 2.0)
(PTHRESH SET1 2.0)
(PTHRESH RESET1 2.0)
(PTHRESH TEMP3 2.0)
(PTHRESH TEMP2 2.0)
(PTHRESH TEMP1 2.0)
(RORIN A1 1)
(RORIN A2 1)
(RORIN B 0.09999999)
(RORIN OUTH 1)
(RORIN OUTL 1)
(RORIN SET3 10)
(RORIN RESET3 10)
(RORIN SET2 10)
(RORIN RESET2 10)
(RORIN SET1 10)
(RORIN RESET1 10)
(RORIN TEMP3 1)
(RORIN TEMP2 1)
(RORIN TEMP1 1)
(VOLTS TEMP3 0.19999997)
(VOLTS SET3 3.4000000)
(VOLTS RESET3 0.20000001)
(VOLTS A1 0.19999999)
(VOLTS A2 0.19999999)
(VOLTS OUTH 0.19999999)
(VOLTS OUTL 3.4000000)
(VOLTS SET2 0.19999999)
(VOLTS RESET2 3.4000000)
(VOLTS SET1 0.19999999)
(VOLTS RESET1 3.4000000)
(VOLTS TEMP2 3.4000000)
(VOLTS TEMP1 3.4000000)
(TYPE A1 SIGNAL)
(TYPE A2 SIGNAL)
(TYPE B SIGNAL)
(TYPE OUTH SIGNAL)
(TYPE OUTL SIGNAL)
(TYPE RINT RES)
(TYPE CEXT CAP)
(TYPE SET3 SIGNAL)
(TYPE RESET3 SIGNAL)
(TYPE SET2 SIGNAL)
(TYPE RESET2 SIGNAL)
(TYPE SET1 SIGNAL)
(TYPE RESET1 SIGNAL)
(TYPE TEMP3 SIGNAL)
(TYPE TEMP2 SIGNAL)
(TYPE TEMP1 SIGNAL)
(TUPLE A2 A1 B OUTH OUTL)
(TUPLE A1 A2 B OUTH OUTL)
(TUPLE RESET1 TEMP1 A1)
(TUPLE SET1 A1 TEMP1)
(TUPLE RESET2 TEMP2 A2)
```

```
(TUPLE SET2 A2 TEMP2)
(TUPLE RESET3 TEMP3 B)
(TUPLE SET3 B TEMP3)
(STATE B HIGH)
(STATE TEMP3 LOW)
(STATE RINT VCC)
(STATE CEXT CLOSED)
(STATE OUT OFF)
(STATE A1 LOW)
(STATE A2 LOW)
(STATE TEMP1 HIGH)
(STATE TEMP2 HIGH)
****SKLRS****
(VOLTS B 1.3579999)
******************

<<<DESTROYING CB>>> TIME = 20.920000
STARTUP ** (S B) (CVOLTS 0.19999999) (CRORIN 0.09999999) (CPTHRESH 1.
5499999)

<<<CREATING CB>>> TIME = 20.920000
FINISHUP ** (S B) (CVOLTS 1.5499999) (CRORIN 0.09999999) (CPTHRESH 1.
5499999)

<<<CREATING CB>>> TIME = 20.920000
TRIGGERB ** (Q A2) (R A1) (S B) (O OUTH) (ONOT OUTL) (CVOLTS 0.199999
99)

<<<DESTROYING CB>>> TIME = 20.920000
TRIGGERB ** (Q A2) (R A1) (S B) (O OUTH) (ONOT OUTL) (CVOLTS 0.199999
99)

<<<CREATING CB>>> TIME = 20.920000
PROPDELAYLH ** (Q B) (L OUTH) (CPLHIN 35) (CRORIN 1) (CVOLTS 0.199999
99) (CPTHRESH 1.4000000)

<<<CREATING CB>>> TIME = 20.920000
PROPDELAYHL ** (Q B) (Z OUTL) (CPHLIN 40) (CRORIN 1) (CVOLTS 3.400000
0) (CNTHRESH 1.4000000)

<<<DESTROYING CB>>> TIME = 30.180000
HIT ** (S SET3) (CNBOUNCE 5)

<<<CREATING CB>>> TIME = 30.180000
STARTDN ** (S SET3) (CVOLTS 3.4000000) (CRORIN 10) (CNTHRESH 0.799999
99)

<<<DESTROYING CB>>> TIME = 30.440000
STARTDN ** (S SET3) (CVOLTS 3.4000000) (CRORIN 10) (CNTHRESH 0.799999
99)

<<<CREATING CB>>> TIME = 30.440000
FINISHDN ** (S SET3) (CVOLTS 0.79999999) (CRORIN 10) (CNTHRESH 0.7999
9999)

<<<CREATING CB>>> TIME = 30.440000
BOUNCE ** (S SET3) (CNBOUNCE 5)

<<<DESTROYING CB>>> TIME = 30.5
FINISHDN ** (S SET3) (CVOLTS 0.79999999) (CRORIN 10) (CNTHRESH 0.7999
9999)
```

```
<<<DESTROYING CB>>> TIME = 35.440000
BOUNCE ** (S SET3) (CNBOUNCE 5)

<<<CREATING CB>>> TIME = 35.440000
STARTUP ** (S SET3) (CVOLTS 0.20000056) (CRORIN 10) (CPTHRESH 2.0)

<<<DESTROYING CB>>> TIME = 35.619999
STARTUP ** (S SET3) (CVOLTS 0.20000056) (CRORIN 10) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 35.619999
FINISHUP ** (S SET3) (CVOLTS 2.0) (CRORIN 10) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 35.619999
HIT ** (S SET3) (CNBOUNCE NEW)

<<<DESTROYING CB>>> TIME = 35.759999
FINISHUP ** (S SET3) (CVOLTS 2.0) (CRORIN 10) (CPTHRESH 2.0)

<<<DESTROYING CB>>> TIME = 39.420000
FINISHUP ** (S B) (CVOLTS 1.5499999) (CRORIN 0.09999999) (CPTHRESH 1.
5499999)

<<<DESTROYING CB>>> TIME = 54.720000
PROPDELAYLH ** (Q B) (L OUTH) (CPLHIN 35) (CRORIN 1) (CVOLTS 0.199999
99) (CPTHRESH 1.4000000)

<<<CREATING CB>>> TIME = 54.720000
STARTUP ** (S OUTH) (CVOLTS 0.19999999) (CRORIN 1) (CPTHRESH 1.400000
0)

<<<DESTROYING CB>>> TIME = 55.920000
STARTUP ** (S OUTH) (CVOLTS 0.19999999) (CRORIN 1) (CPTHRESH 1.400000
0)

<<<CREATING CB>>> TIME = 55.920000
FINISHUP ** (S OUTH) (CVOLTS 1.4000000) (CRORIN 1) (CPTHRESH 1.400000
0)

<<<DESTROYING CB>>> TIME = 57.920000
FINISHUP ** (S OUTH) (CVOLTS 1.4000000) (CRORIN 1) (CPTHRESH 1.400000
0)

<<<CREATING CB>>> TIME = 57.920000
OUTPUTHIGH ** (A A2) (B A1) (G B) (Q OUTH) (D OUTL) (R RINT) (C CEXT)
 (CRORIN 1) (CVOLTS 3.4000000) (CRSIZE 2) (CSIZE 30)

<<<DESTROYING CB>>> TIME = 58.920000
PROPDELAYHL ** (Q B) (Z OUTL) (CPHLIN 40) (CRORIN 1) (CVOLTS 3.400000
0) (CNTHRESH 1.4000000)

<<<CREATING CB>>> TIME = 58.920000
STARTDN ** (S OUTL) (CVOLTS 3.4000000) (CRORIN 1) (CNTHRESH 1.4000000
)

<<<DESTROYING CB>>> TIME = 60.920000
STARTDN ** (S OUTL) (CVOLTS 3.4000000) (CRORIN 1) (CNTHRESH 1.4000000
)
```

```
<<<CREATING CB>>> TIME = 60.920000
FINISHDN ** (S OUTL) (CVOLTS 1.4000000) (CRORIN 1) (CNTHRESH 1.400000
0)

<<<DESTROYING CB>>> TIME = 62.119999
FINISHDN ** (S OUTL) (CVOLTS 1.4000000) (CRORIN 1) (CNTHRESH 1.400000
0)

<<<CREATING CB>>> TIME = 62.119999
OUTPUTLOW ** (A A2) (B A1) (G B) (D OUTH) (Q OUTL) (R RINT) (C CEXT)
(CRORIN 1) (CVOLTS 0.20000019) (CRSIZE 2) (CSIZE 30)

<<<DESTROYING CB>>> TIME = 65.619999
HIT ** (S SET3) (CNBOUNCE NEW)

<<<CREATING CB>>> TIME = 65.619999
STARTDN ** (S SET3) (CVOLTS 3.3999986) (CRORIN 10) (CNTHRESH 0.799999
99)

<<<DESTROYING CB>>> TIME = 65.880000
STARTDN ** (S SET3) (CVOLTS 3.3999986) (CRORIN 10) (CNTHRESH 0.799999
99)

<<<CREATING CB>>> TIME = 65.880000
FINISHDN ** (S SET3) (CVOLTS 0.79999999) (CRORIN 10) (CNTHRESH 0.7999
9999)

<<<CREATING CB>>> TIME = 65.880000
BOUNCE ** (S SET3) (CNBOUNCE NEW)

<<<DESTROYING CB>>> TIME = 65.940000
FINISHDN ** (S SET3) (CVOLTS 0.79999999) (CRORIN 10) (CNTHRESH 0.7999
9999)

<<<DESTROYING CB>>> TIME = 68.880000
BOUNCE ** (S SET3) (CNBOUNCE NEW)

<<<CREATING CB>>> TIME = 68.880000
STARTUP ** (S SET3) (CVOLTS 0.19999580) (CRORIN 10) (CPTHRESH 2.0)

<<<DESTROYING CB>>> TIME = 69.060000
STARTUP ** (S SET3) (CVOLTS 0.19999580) (CRORIN 10) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 69.060000
FINISHUP ** (S SET3) (CVOLTS 2.0) (CRORIN 10) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 69.060000
HIT ** (S SET3) (CNBOUNCE NEW)

<<<DESTROYING CB>>> TIME = 69.200000
FINISHUP ** (S SET3) (CVOLTS 2.0) (CRORIN 10) (CPTHRESH 2.0)

****TIME****
90
****EXPRS****
(UP RESET3 SET3 SW3)
(RSIZE RINT 2)
(SIZE CEXT 30)
(NBOUNCE SET3 NEW)
(NBOUNCE RESET3 0)
```

```
(NBOUNCE SET2 0)
(NBOUNCE RESET2 0)
(NBOUNCE SET1 0)
(NBOUNCE RESET1 0)
(CONTACT SET3 ON)
(CONTACT RESET3 OFF)
(CONTACT SET2 OFF)
(CONTACT RESET2 ON)
(CONTACT SET1 OFF)
(CONTACT RESET1 ON)
(DOWN RESET2 SET2 SW2)
(DOWN RESET1 SET1 SW1)
(PHLIN A1 50)
(PHLIN A2 50)
(PHLIN B 40)
(PHLIN OUTH 0)
(PHLIN OUTL 0)
(PHLIN SET3 8)
(PHLIN RESET3 8)
(PHLIN SET2 8)
(PHLIN RESET2 8)
(PHLIN SET1 8)
(PHLIN RESET1 8)
(PHLIN TEMP3 0)
(PHLIN TEMP2 0)
(PHLIN TEMP1 0)
(PLHIN A1 45)
(PLHIN A2 45)
(PLHIN B 35)
(PLHIN OUTH 0)
(PLHIN OUTL 0)
(PLHIN SET3 12)
(PLHIN RESET3 12)
(PLHIN SET2 12)
(PLHIN RESET2 12)
(PLHIN SET1 12)
(PLHIN RESET1 12)
(PLHIN TEMP3 0)
(PLHIN TEMP2 0)
(PLHIN TEMP1 0)
(PULSEDN SET3 OFF)
(PULSEDN OUTL OFF)
(PULSEDN TEMP3 OFF)
(PULSEDN RESET3 OFF)
(PULSEDN A1 OFF)
(PULSEDN A2 OFF)
(PULSEDN B OFF)
(PULSEDN OUTH OFF)
(PULSEDN SET2 OFF)
(PULSEDN RESET2 OFF)
(PULSEDN SET1 OFF)
(PULSEDN RESET1 OFF)
(PULSEDN TEMP2 OFF)
(PULSEDN TEMP1 OFF)
(PULSEUP SET3 OFF)
(PULSEUP OUTH OFF)
(PULSEUP B OFF)
(PULSEUP A1 OFF)
(PULSEUP A2 OFF)
(PULSEUP OUTL OFF)
```

```
(PULSEUP RESET3 OFF)
(PULSEUP SET2 OFF)
(PULSEUP RESET2 OFF)
(PULSEUP SET1 OFF)
(PULSEUP RESET1 OFF)
(PULSEUP TEMP3 OFF)
(PULSEUP TEMP2 OFF)
(PULSEUP TEMP1 OFF)
(NTHRESH A1 1.4000000)
(NTHRESH A2 1.4000000)
(NTHRESH B 1.3500000)
(NTHRESH OUTH 1.4000000)
(NTHRESH OUTL 1.4000000)
(NTHRESH SET3 0.79999999)
(NTHRESH RESET3 0.79999999)
(NTHRESH SET2 0.79999999)
(NTHRESH RESET2 0.79999999)
(NTHRESH SET1 0.79999999)
(NTHRESH RESET1 0.79999999)
(NTHRESH TEMP3 0.79999999)
(NTHRESH TEMP2 0.79999999)
(NTHRESH TEMP1 0.79999999)
(PTHRESH A1 1.4000000)
(PTHRESH A2 1.4000000)
(PTHRESH B 1.5499999)
(PTHRESH OUTH 1.4000000)
(PTHRESH OUTL 1.4000000)
(PTHRESH SET3 2.0)
(PTHRESH RESET3 2.0)
(PTHRESH SET2 2.0)
(PTHRESH RESET2 2.0)
(PTHRESH SET1 2.0)
(PTHRESH RESET1 2.0)
(PTHRESH TEMP3 2.0)
(PTHRESH TEMP2 2.0)
(PTHRESH TEMP1 2.0)
(RORIN A1 1)
(RORIN A2 1)
(RORIN B 0.09999999)
(RORIN OUTH 1)
(RORIN OUTL 1)
(RORIN SET3 10)
(RORIN RESET3 10)
(RORIN SET2 10)
(RORIN RESET2 10)
(RORIN SET1 10)
(RORIN RESET1 10)
(RORIN TEMP3 1)
(RORIN TEMP2 1)
(RORIN TEMP1 1)
(VOLTS SET3 3.4000034)
(VOLTS OUTL 0.20000019)
(VOLTS OUTH 3.4000000)
(VOLTS B 3.4000000)
(VOLTS TEMP3 0.19999997)
(VOLTS RESET3 0.20000001)
(VOLTS A1 0.19999999)
(VOLTS A2 0.19999999)
(VOLTS SET2 0.19999999)
(VOLTS RESET2 3.4000000)
```

```
(VOLTS SET1 0.19999999)
(VOLTS RESET1 3.4000000)
(VOLTS TEMP2 3.4000000)
(VOLTS TEMP1 3.4000000)
(TYPE A1 SIGNAL)
(TYPE A2 SIGNAL)
(TYPE B SIGNAL)
(TYPE OUTH SIGNAL)
(TYPE OUTL SIGNAL)
(TYPE RINT RES)
(TYPE CEXT CAP)
(TYPE SET3 SIGNAL)
(TYPE RESET3 SIGNAL)
(TYPE SET2 SIGNAL)
(TYPE RESET2 SIGNAL)
(TYPE SET1 SIGNAL)
(TYPE RESET1 SIGNAL)
(TYPE TEMP3 SIGNAL)
(TYPE TEMP2 SIGNAL)
(TYPE TEMP1 SIGNAL)
(TUPLE A2 A1 B OUTH OUTL)
(TUPLE A1 A2 B OUTH OUTL)
(TUPLE RESET1 TEMP1 A1)
(TUPLE SET1 A1 TEMP1)
(TUPLE RESET2 TEMP2 A2)
(TUPLE SET2 A2 TEMP2)
(TUPLE RESET3 TEMP3 B)
(TUPLE SET3 B TEMP3)
(STATE OUT ON)
(STATE B HIGH)
(STATE TEMP3 LOW)
(STATE RINT VCC)
(STATE CEXT CLOSED)
(STATE A1 LOW)
(STATE A2 LOW)
(STATE TEMP1 HIGH)
(STATE TEMP2 HIGH)
****SKLRS****
*****************

<<<DESTROYING CB>>> TIME = 99.060000
HIT ** (S SET3) (CNBOUNCE NEW)

<<<CREATING CB>>> TIME = 99.060000
STARTDN ** (S SET3) (CVOLTS 3.4000034) (CRORIN 10) (CNTHRESH 0.799999
99)

<<<DESTROYING CB>>> TIME = 99.320000
STARTDN ** (S SET3) (CVOLTS 3.4000034) (CRORIN 10) (CNTHRESH 0.799999
99)

<<<CREATING CB>>> TIME = 99.320000
FINISHDN ** (S SET3) (CVOLTS 0.79999999) (CRORIN 10) (CNTHRESH 0.7999
9999)

<<<CREATING CB>>> TIME = 99.320000
BOUNCE ** (S SET3) (CNBOUNCE NEW)

<<<DESTROYING CB>>> TIME = 99.380001
FINISHDN ** (S SET3) (CVOLTS 0.79999999) (CRORIN 10) (CNTHRESH 0.7999
9999)
```

```
<<<DESTROYING CB>>> TIME = 101.32000
BOUNCE ** (S SET3) (CNBOUNCE NEW)

<<<CREATING CB>>> TIME = 101.32000
STARTUP ** (S SET3) (CVOLTS 0.19999580) (CRORIN 10) (CPTHRESH 2.0)

<<<DESTROYING CB>>> TIME = 101.50000
STARTUP ** (S SET3) (CVOLTS 0.19999580) (CRORIN 10) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 101.50000
FINISHUP ** (S SET3) (CVOLTS 2.0) (CRORIN 10) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 101.50000
HIT ** (S SET3) (CNBOUNCE NEW)

<<<DESTROYING CB>>> TIME = 101.64000
FINISHUP ** (S SET3) (CVOLTS 2.0) (CRORIN 10) (CPTHRESH 2.0)

<<<DESTROYING CB>>> TIME = 114.72000
OUTPUTHIGH ** (A A2) (B A1) (G B) (Q OUTH) (D OUTL) (R RINT) (C CEXT)
 (CRORIN 1) (CVOLTS 3.4000000) (CRSIZE 2) (CSIZE 30)

<<<CREATING CB>>> TIME = 114.72000
STARTDN ** (S OUTH) (CVOLTS 3.4000000) (CRORIN 1) (CNTHRESH 1.4000000
)

<<<DESTROYING CB>>> TIME = 116.72000
STARTDN ** (S OUTH) (CVOLTS 3.4000000) (CRORIN 1) (CNTHRESH 1.4000000
)

<<<CREATING CB>>> TIME = 116.72000
FINISHDN ** (S OUTH) (CVOLTS 1.4000000) (CRORIN 1) (CNTHRESH 1.400000
0)

<<<DESTROYING CB>>> TIME = 117.92000
FINISHDN ** (S OUTH) (CVOLTS 1.4000000) (CRORIN 1) (CNTHRESH 1.400000
0)

<<<DESTROYING CB>>> TIME = 118.92000
OUTPUTLOW ** (A A2) (B A1) (G B) (D OUTH) (Q OUTL) (R RINT) (C CEXT)
(CRORIN 1) (CVOLTS 0.20000019) (CRSIZE 2) (CSIZE 30)

<<<CREATING CB>>> TIME = 118.92000
STARTUP ** (S OUTL) (CVOLTS 0.20000019) (CRORIN 1) (CPTHRESH 1.400000
0)

<<<DESTROYING CB>>> TIME = 120.11999
STARTUP ** (S OUTL) (CVOLTS 0.20000019) (CRORIN 1) (CPTHRESH 1.400000
0)

<<<CREATING CB>>> TIME = 120.11999
FINISHUP ** (S OUTL) (CVOLTS 1.4000000) (CRORIN 1) (CPTHRESH 1.400000
0)

<<<DESTROYING CB>>> TIME = 122.11999
FINISHUP ** (S OUTL) (CVOLTS 1.4000000) (CRORIN 1) (CPTHRESH 1.400000
0)
```

```
<<<DESTROYING CB>>> TIME = 131.50000
HIT ** (S SET3) (CNBOUNCE NEW)

<<<CREATING CB>>> TIME = 131.50000
STARTDN ** (S SET3) (CVOLTS 3.4000034) (CRORIN 10) (CNTHRESH 0.799999
99)

<<<DESTROYING CB>>> TIME = 131.76000
STARTDN ** (S SET3) (CVOLTS 3.4000034) (CRORIN 10) (CNTHRESH 0.799999
99)

<<<CREATING CB>>> TIME = 131.76000
FINISHDN ** (S SET3) (CVOLTS 0.79999999) (CRORIN 10) (CNTHRESH 0.7999
9999)

<<<CREATING CB>>> TIME = 131.76000
BOUNCE ** (S SET3) (CNBOUNCE NEW)

<<<DESTROYING CB>>> TIME = 131.82000
FINISHDN ** (S SET3) (CVOLTS 0.79999999) (CRORIN 10) (CNTHRESH 0.7999
9999)

<<<DESTROYING CB>>> TIME = 132.76000
BOUNCE ** (S SET3) (CNBOUNCE NEW)

<<<CREATING CB>>> TIME = 132.76000
STARTUP ** (S SET3) (CVOLTS 0.20000533) (CRORIN 10) (CPTHRESH 2.0)

<<<DESTROYING CB>>> TIME = 132.94000
STARTUP ** (S SET3) (CVOLTS 0.20000533) (CRORIN 10) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 132.94000
FINISHUP ** (S SET3) (CVOLTS 2.0) (CRORIN 10) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 132.94000
HIT ** (S SET3) (CNBOUNCE NEW)

<<<DESTROYING CB>>> TIME = 133.08000
FINISHUP ** (S SET3) (CVOLTS 2.0) (CRORIN 10) (CPTHRESH 2.0)

<<<DESTROYING CB>>> TIME = 162.94000
HIT ** (S SET3) (CNBOUNCE NEW)

<<<CREATING CB>>> TIME = 162.94000
STARTDN ** (S SET3) (CVOLTS 3.3999938) (CRORIN 10) (CNTHRESH 0.799999
99)

<<<DESTROYING CB>>> TIME = 163.20000
STARTDN ** (S SET3) (CVOLTS 3.3999938) (CRORIN 10) (CNTHRESH 0.799999
99)

<<<CREATING CB>>> TIME = 163.20000
FINISHDN ** (S SET3) (CVOLTS 0.79999999) (CRORIN 10) (CNTHRESH 0.7999
9999)

<<<CREATING CB>>> TIME = 163.20000
BOUNCE ** (S SET3) (CNBOUNCE NEW)

<<<DESTROYING CB>>> TIME = 163.20000
BOUNCE ** (S SET3) (CNBOUNCE NEW)
```

```
<<<DESTROYING CB>>> TIME = 163.26000
FINISHDN ** (S SET3) (CVOLTS 0.79999999) (CRORIN 10) (CNTHRESH 0.7999
9999)

<<<CREATING CB>>> TIME = 163.26000
STARTUP ** (S SET3) (CVOLTS 0.20000533) (CRORIN 10) (CPTHRESH 2.0)

<<<DESTROYING CB>>> TIME = 163.44000
STARTUP ** (S SET3) (CVOLTS 0.20000533) (CRORIN 10) (CPTHRESH 2.0)

<<<CREATING CB>>> TIME = 163.44000
FINISHUP ** (S SET3) (CVOLTS 2.0) (CRORIN 10) (CPTHRESH 2.0)

<<<DESTROYING CB>>> TIME = 163.58000
FINISHUP ** (S SET3) (CVOLTS 2.0) (CRORIN 10) (CPTHRESH 2.0)

COMMAND: *PICTURE


****TIME****
163.58000
****EXPRS****
(UP RESET3 SET3 SW3)
(RSIZE RINT 2)
(SIZE CEXT 30)
(LEFTIN OUTL ZERO)
(LEFTIN OUTH ZERO)
(NBOUNCE SET3 NEW)
(NBOUNCE RESET3 0)
(NBOUNCE SET2 0)
(NBOUNCE RESET2 0)
(NBOUNCE SET1 0)
(NBOUNCE RESET1 0)
(CONTACT SET3 ON)
(CONTACT RESET3 OFF)
(CONTACT SET2 OFF)
(CONTACT RESET2 ON)
(CONTACT SET1 OFF)
(CONTACT RESET1 ON)
(DOWN RESET2 SET2 SW2)
(DOWN RESET1 SET1 SW1)
(PHLIN A1 50)
(PHLIN A2 50)
(PHLIN B 40)
(PHLIN OUTH 0)
(PHLIN OUTL 0)
(PHLIN SET3 8)
(PHLIN RESET3 8)
(PHLIN SET2 8)
(PHLIN RESET2 8)
(PHLIN SET1 8)
(PHLIN RESET1 8)
(PHLIN TEMP3 0)
(PHLIN TEMP2 0)
(PHLIN TEMP1 0)
(PLHIN A1 45)
(PLHIN A2 45)
(PLHIN B 35)
(PLHIN OUTH 0)
(PLHIN OUTL 0)
```

```
(PLHIN SET3 12)
(PLHIN RESET3 12)
(PLHIN SET2 12)
(PLHIN RESET2 12)
(PLHIN SET1 12)
(PLHIN RESET1 12)
(PLHIN TEMP3 0)
(PLHIN TEMP2 0)
(PLHIN TEMP1 0)
(PULSEDN SET3 OFF)
(PULSEDN OUTH OFF)
(PULSEDN OUTL OFF)
(PULSEDN TEMP3 OFF)
(PULSEDN RESET3 OFF)
(PULSEDN A1 OFF)
(PULSEDN A2 OFF)
(PULSEDN B OFF)
(PULSEDN SET2 OFF)
(PULSEDN RESET2 OFF)
(PULSEDN SET1 OFF)
(PULSEDN RESET1 OFF)
(PULSEDN TEMP2 OFF)
(PULSEDN TEMP1 OFF)
(PULSEUP SET3 OFF)
(PULSEUP OUTL OFF)
(PULSEUP OUTH OFF)
(PULSEUP B OFF)
(PULSEUP A1 OFF)
(PULSEUP A2 OFF)
(PULSEUP RESET3 OFF)
(PULSEUP SET2 OFF)
(PULSEUP RESET2 OFF)
(PULSEUP SET1 OFF)
(PULSEUP RESET1 OFF)
(PULSEUP TEMP3 OFF)
(PULSEUP TEMP2 OFF)
(PULSEUP TEMP1 OFF)
(NTHRESH A1 1.4000000)
(NTHRESH A2 1.4000000)
(NTHRESH B 1.3500000)
(NTHRESH OUTH 1.4000000)
(NTHRESH OUTL 1.4000000)
(NTHRESH SET3 0.79999999)
(NTHRESH RESET3 0.79999999)
(NTHRESH SET2 0.79999999)
(NTHRESH RESET2 0.79999999)
(NTHRESH SET1 0.79999999)
(NTHRESH RESET1 0.79999999)
(NTHRESH TEMP3 0.79999999)
(NTHRESH TEMP2 0.79999999)
(NTHRESH TEMP1 0.79999999)
(PTHRESH A1 1.4000000)
(PTHRESH A2 1.4000000)
(PTHRESH B 1.5499999)
(PTHRESH OUTH 1.4000000)
(PTHRESH OUTL 1.4000000)
(PTHRESH SET3 2.0)
(PTHRESH RESET3 2.0)
(PTHRESH SET2 2.0)
(PTHRESH RESET2 2.0)
```

```
(PTHRESH SET1 2.0)
(PTHRESH RESET1 2.0)
(PTHRESH TEMP3 2.0)
(PTHRESH TEMP2 2.0)
(PTHRESH TEMP1 2.0)
(RORIN A1 1)
(RORIN A2 1)
(RORIN B 0.09999999)
(RORIN OUTH 1)
(RORIN OUTL 1)
(RORIN SET3 10)
(RORIN RESET3 10)
(RORIN SET2 10)
(RORIN RESET2 10)
(RORIN SET1 10)
(RORIN RESET1 10)
(RORIN TEMP3 1)
(RORIN TEMP2 1)
(RORIN TEMP1 1)
(VOLTS SET3 3.3999938)
(VOLTS OUTL 3.4000000)
(VOLTS OUTH 0.20000019)
(VOLTS B 3.4000000)
(VOLTS TEMP3 0.19999997)
(VOLTS RESET3 0.20000001)
(VOLTS A1 0.19999999)
(VOLTS A2 0.19999999)
(VOLTS SET2 0.19999999)
(VOLTS RESET2 3.4000000)
(VOLTS SET1 0.19999999)
(VOLTS RESET1 3.4000000)
(VOLTS TEMP2 3.4000000)
(VOLTS TEMP1 3.4000000)
(TYPE A1 SIGNAL)
(TYPE A2 SIGNAL)
(TYPE B SIGNAL)
(TYPE OUTH SIGNAL)
(TYPE OUTL SIGNAL)
(TYPE RINT RES)
(TYPE CEXT CAP)
(TYPE SET3 SIGNAL)
(TYPE RESET3 SIGNAL)
(TYPE SET2 SIGNAL)
(TYPE RESET2 SIGNAL)
(TYPE SET1 SIGNAL)
(TYPE RESET1 SIGNAL)
(TYPE TEMP3 SIGNAL)
(TYPE TEMP2 SIGNAL)
(TYPE TEMP1 SIGNAL)
(TUPLE A2 A1 B OUTH OUTL)
(TUPLE A1 A2 B OUTH OUTL)
(TUPLE RESET1 TEMP1 A1)
(TUPLE SET1 A1 TEMP1)
(TUPLE RESET2 TEMP2 A2)
(TUPLE SET2 A2 TEMP2)
(TUPLE RESET3 TEMP3 B)
(TUPLE SET3 B TEMP3)
(STATE OUT OFF)
(STATE B HIGH)
(STATE TEMP3 LOW)
```

```
(STATE RINT VCC)
(STATE CEXT CLOSED)
(STATE A1 LOW)
(STATE A2 LOW)
(STATE TEMP1 HIGH)
(STATE TEMP2 HIGH)
****SKLRS****
****************

COMMAND: *STOP

(****TERMINATED-AT-TIME**** 163.58000)

.
```

10. Conclusion

Hendrix's system has previously been used primarily to model events on a large scale, with time measured in minutes or in seconds. We have shown that this model will also accurately simulate events which take place on a very short time scale. Since our models of digital circuits are accurate, this system could, then, be a powerful tool for teaching digital electronics. When writing scenarios for any circuit, the student must first understand the operation of each part, and must also understand the interrelationships of all the components in the circuit.

Gary Hendrix's ideas are embodied in CONCUR, a language for continuous, concurrent processes [1], which is currently being implemented at Indiana University.

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