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Area-Efficient Implication Circuits for Very Dense Łukasiewicz Logic Arrays

by

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Abstract

A one-diode circuit for negated implication ($\not\supset$) is derived from a 12-transistor Łukasiewicz implication circuit ($\supset$). The derivation also yields an adjustable three-transistor implication circuit with maximum error less than 1% of full scale. Two Łukasiewicz logic arrays (ŁLAs) are proposed that use area-efficient implementations of the one-diode and three-transistor implication circuits. The very dense diode-tower ŁLA contains 36,000 implications in an area that previously held 92 implications; the three-transistor ŁLA contains 1,990 implications. Both ŁLAs double the number of inputs per pin on the IC package. Very dense ŁLAs make ŁLA-based fuzzy controllers and neural networks practical.

1. INTRODUCTION

1.1 ŁUKASIEWICZ LOGIC AND ELECTRONIC CIRCUITS

Continuous-valued analog circuits for Łukasiewicz implication ($\supset$) and negated implication ($\not\supset$) are the basis for analog array processors called *Łukasiewicz logic arrays (ŁLAs)* [1].

Łukasiewicz logic (Ł) has a denumerably infinite number of truth values [2].[1] Ł describes the class of ideal analog circuits that have an infinite maximum precision (Figure 1). Real analog circuits, which have a finite maximum precision, are classified by the number of data values encoded on individual wires in the circuit. A circuit is described by a subset of Ł designated as Ł_n, where n specifies a whole number of truth values.

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[1] Ł_1 is replaced by Ł to avoid confusion when using Ł_n to denote subsets of Ł_1.

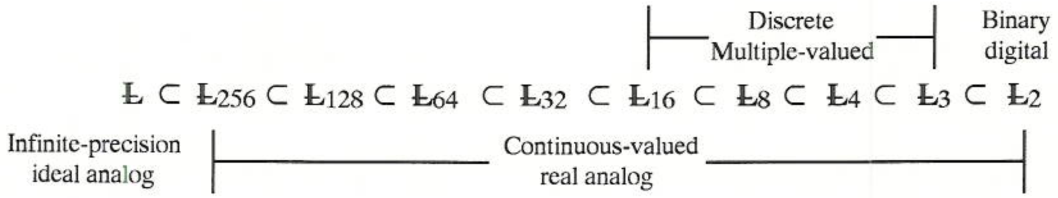

Discrete
Multiple-valued
Binary
digital
$\text{Ł} \subset \text{Ł}_{256} \subset \text{Ł}_{128} \subset \text{Ł}_{64} \subset \text{Ł}_{32} \subset \text{Ł}_{16} \subset \text{Ł}_{8} \subset \text{Ł}_{4} \subset \text{Ł}_{3} \subset \text{Ł}_{2}$
Infinite-precision
ideal analog
Continuous-valued
real analog

Figure 1. Relationship between Łukasiewicz logic and electronic circuits.

Ł_2 is the most familiar subset of Ł: it is the Boolean logic that describes binary digital circuits. Discrete multiple-valued circuits are described by subsets of Ł with $2 < n \leq 16$. Continuous-valued analog circuits are described by subsets of Ł with $2 \leq n \leq 2^p$, where p is the maximum precision of the circuit in bits. Typically p falls in the range $6 \leq p \leq 12$.

Continuous-valued analog ŁLAs have a dual logical and algebraic semantics that makes them capable of both symbolic and numeric computation. Fuzzy controllers, neural networks, inference engines and general-purpose analog computers (GPACs) can be implemented with ŁLAs.

1.2 ŁUKASIEWICZ LOGIC ARRAYS

An ŁLA is organized as an H-tree array that implements a sentence schema of Ł. The processing elements of the ŁLA correspond to implications or negated implications in the sentence schema (Figure 2). *Łukasiewicz implication* is defined by the valuation function $v(\alpha \supset \beta) = min(\ 1,\ 1-\alpha+\beta\ )$. *Negated implication* has a valuation function defined as $v(\alpha \not\supset \beta) = max(\ 0,\ \alpha-\beta\ )$. Negated implication is identical to bounded difference ($\ominus$) [3], but indicates its relation to implication: $\not\supset \equiv \neg\ (\alpha \supset \beta)$. The term *implication* is occasionally used to refer to both functions.

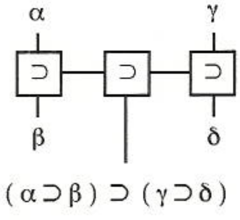


Figure 2. ŁLA H-tree corresponds to binary-tree-structured sentence schema.

Two implication circuits are described in this paper. The first is a one-diode negated implication circuit. The second is a three-transistor implication circuit with trim inputs that reduce error to less than 1% of full scale. Both circuits are derived from a 12-transistor Łukasiewicz implication circuit (ŁL9 implication). Two Łukasiewicz logic arrays (ŁLAs) are proposed that use area-efficient implementations of the one-diode and three-transistor implication circuits. The *diode tower* is introduced to implement very dense ŁLAs. It is a three-dimensional VLSI structure composed of a vertically-stacked pair of Schottky-diode negated-implication circuits.

1.3 ADVANTAGES AND DISADVANTAGES OF VERY DENSE ŁLAS

Diode-tower and three-transistor ŁLAs contain more implications than previous ŁLAs. The diode-tower ŁLA is estimated to contain 36,000 implications in 1800μ × 2000μ, the area of a MOSIS Tiny Chip. Using the ŁL9 implication cell the same area contains a maximum of 92 implications. The diode-tower ŁLA is as accurate as ŁL9, the prototype ŁLA that used the 12-transistor implication circuit.

The three-transistor ŁLA can be fabricated using nMOS current mirrors alone. The resulting array is less dense than the diode-tower ŁLA, but does not require the special process technology needed to fabricate diode towers. The three-transistor ŁLA contains a maximum of 1,990 implications in an 1800μ × 2000μ area, and is more accurate than ŁL9. The maximum error of the three-transistor ŁLA with trim inputs is 0.8% of full scale, while the maximum error for ŁL9 is 4% of full scale [4].

Both ŁLAs have the additional advantage that array inputs are the difference of two currents. This allows two input values for each input pin on the ŁLA integrated circuit package. However, even with twice the number of input values, ŁLAs are pin-limited devices. Application architectures must have numerous internal connections to fully utilize very dense ŁLAs.

1.4 APPLICATION ARCHITECTURES REQUIRE VERY DENSE ŁLAS

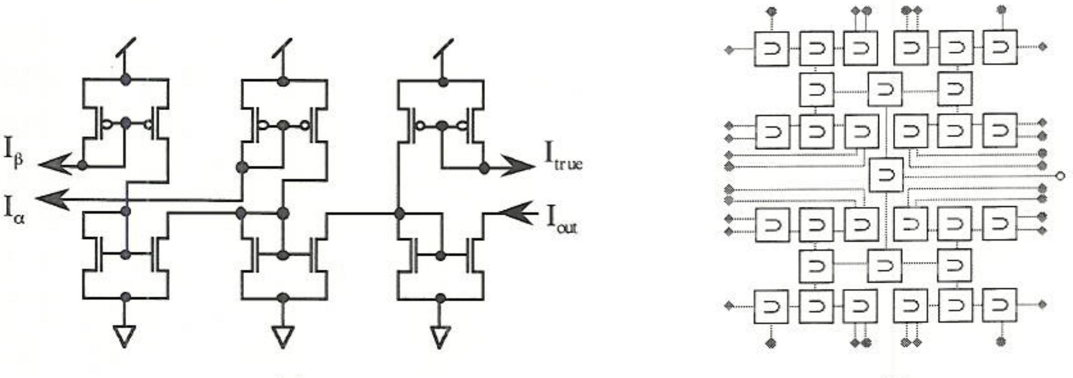
Applications for Łukasiewicz logic arrays include fuzzy controllers, neural networks, tautology checkers for Ł, and general-purpose analog computers (GPACs) [5, 6, 7, 8, 9]. Arithmetic and logical functions are defined using implication or negated implication [3, 6]. A specific processor is constructed by mapping arithmetic and logical functions with varied precision to one or more ŁLAs [1, 3, 6, 7].

Architectures for these applications can not be implemented with the prototype ŁLAs, which contain too few implications. The Achernar ŁLA compiler typically outputs sentences containing hundreds of implications, with many internal and few external connections [10]. ŁL9, the prototype ŁLA, has only 32 implications per chip [4]. Practical architectures built with ŁLAs require at least 1,000 implications on a chip. ŁLAs of this density can be built with the area-efficient implication and negated implication circuits described in this paper.

2. AREA-EFFICIENT ANALOG CIRCUITS FOR ŁUKASIEWICZ IMPLICATION

2.1 DERIVING THREE-TRANSISTOR AND ONE-DIODE IMPLICATION CIRCUITS

The ŁL9 Łukasiewicz implication cell is based on an earlier design that implemented negation and implication using Yamakawa's basic fuzzy logic cell [11]. The earlier design is simplified in ŁL9 to an implication cell with buffered input currents (Figure 3a). One ŁL9 array contains 32 implication cells (Figure 3b). Negation is programmed at the circuit's inputs by replacing the expression $\neg\alpha$ with the equivalent expression $\alpha \supset F$.



(a) (b)

Figure 3. 12-transistor implication cell (⊃) and ŁL9.

The 12-transistor implication cell of Figure 3a is unnecessarily complex compared to Yamakawa's six-transistor implication cell [3, 11] (Figure 4). However, a three-transistor implication cell and a one-diode negated implication cell (equivalent to Yamakawa's three-transistor bounded difference circuit) can be derived from the 12-transistor cell by removing redundant input buffers, and pairing implications in the array.

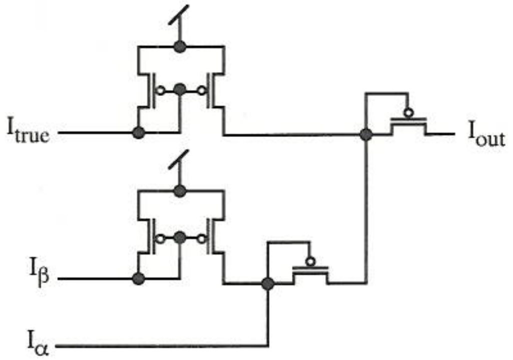
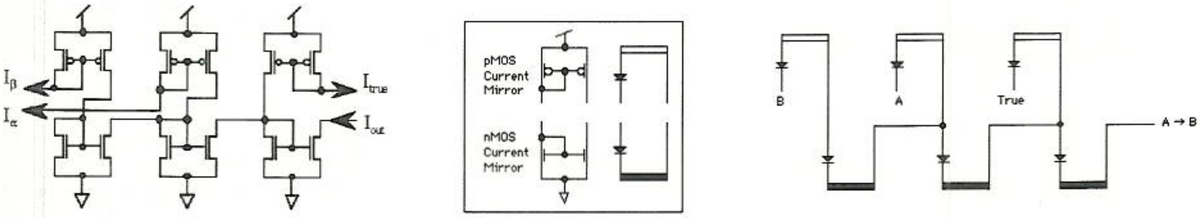


Figure 4. Six-transistor implication cell (⊃).

New schematic symbols are introduced to illustrate the derivation of the three-transistor and one-diode implication cells. The symbols simplify the schematic of ŁL9 implication (Figure 5a). The pMOS and nMOS current mirrors are represented by U-shaped boxes, indicating their function as either current sources or current sinks (Figure 5b). An open bar at the top, like the bubble of a p-transistor, indicates a pMOS current mirror. A solid bar at the bottom indicates an nMOS current mirror. Diode-connected transistors are indicated by a diode. The resulting schematic for ŁL9 implication clearly shows its structure and operation (Figure 5c).

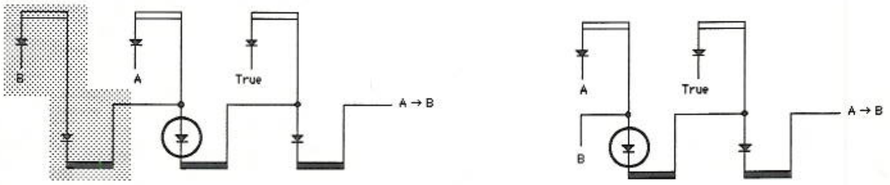


(a) (b) (c)

Figure 5. Original and simplified schematic of the ŁL9 stand-alone implication cell (⊃).

2.1.1 REMOVING UNNECESSARY CURRENT BUFFERS

ŁL9 buffers the β input current before it is subtracted from the buffered α input current (Figure 6a, shaded). Buffering the β input in a binary tree array is redundant because no output drives more than one input. The current-mirror buffers for β also limit the value of β to the interval [0,1]. This is unnecessary because the diode-connected MOSFET (Figure 6, circled) keeps α–β positive. The difference α–β will fall within the interval [0,1] if the inputs α and β lie in the interval [0,1]. Given this constraint, the β current-mirror buffers can be safely removed to yield an eight-transistor implication circuit (Figure 6b).



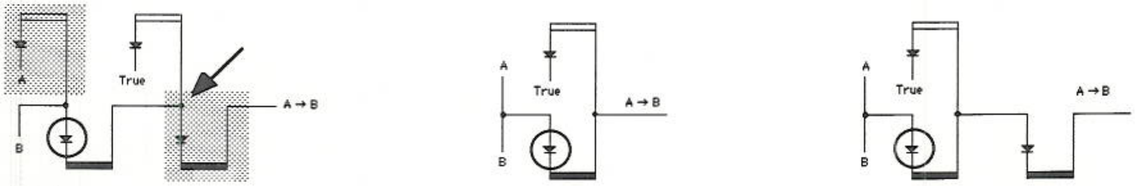
(a) ŁL9 implication (b) Eight-transistor implication

Figure 6. Removing redundant β current mirrors.

2.1.2 SIMPLIFYING IMPLICATION IN AN ARRAY

The α input of the eight-transistor implication circuit is mirrored only to invert the direction of the current flow, allowing implication cells to be connected into an array. However, pairing a current source for α with a current sink for β in the array removes the need for the α input current mirror. The implication cells can then be simplified as a pair.

The current-source cell of the implication pair is derived by eliminating the α input current mirror and the current mirror that provides a current sink at the output (Figure 7a, shaded). The output of the cell becomes a current source (Figure 7b). The current-sink cell of the implication pair is derived by eliminating the α input current mirror alone. The output of the cell is a current sink (Figure 7c).



(a) Eight-transistor implication (b) Current-source cell (c) Current-sink cell

Figure 7. Deriving the current source and current sink cells.

In both cells the circled diode-connected MOSFET computes *max(0, α–β)*. At the node pointed to by the arrow *true – max(0, α–β)* is computed according to Kirchoff's Law. Because α and β are constrained to lie in the interval [0,1] this is equivalent to *min(true, true – α + β)),* the valuation function for implication.

The current-source and current-sink cells are combined into an implication pair. Within the array, one child implication pair is connected to one input of the parent implication pair by a single wire. The wire carries a current whose value is α–β, where α is the output of the child's current-source cell and β is the output of the child's current-sink cell (Figure 8).

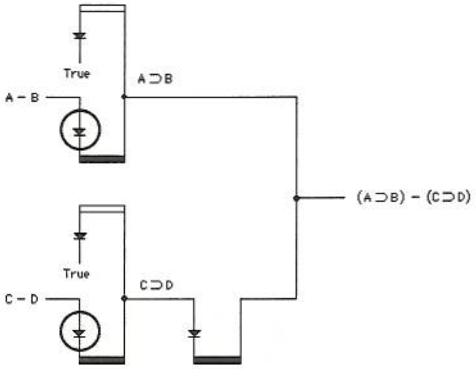
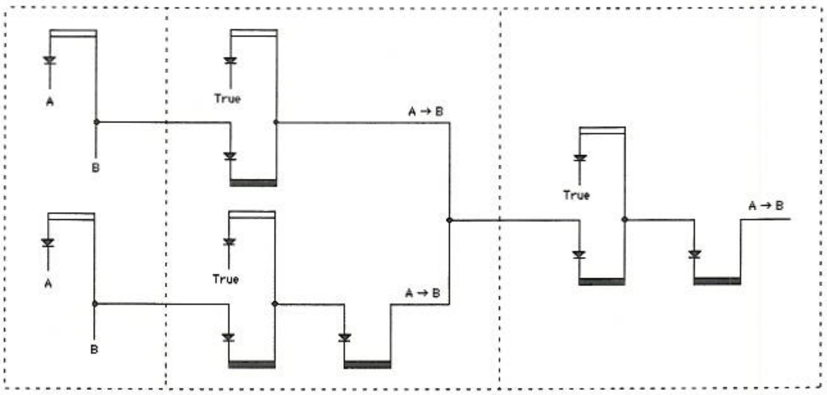


Figure 8. Paired implication averages five transistors per implication circuit.



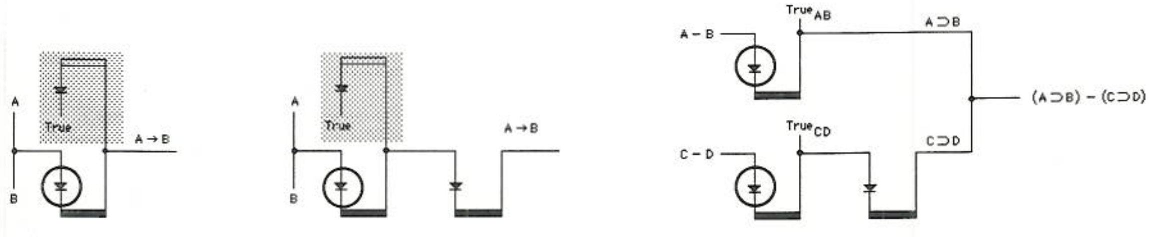
Input cells Interior nodes Root output

Figure 9. Internal components of ŁLA using paired implication.

ŁLAs built from implication pairs have three internal components: input cells, interior paired-implication cells, and a root cell whose output is a current-sink cell (Figure 9). *Input cells* at the leaves of the array are driven by current sinks. The β input is a current sink, but the α input must be inverted with a current mirror to provide a current source. *Interior nodes* of the binary tree are composed of paired implication cells. The *root output* is a current-sink implication cell because its output is used directly. When cascading ŁLAs, the difference between the outputs of two lower-level ŁLAs is computed by the input cell of the next-higher ŁLA.

2.1.3 THREE-TRANSISTOR IMPLICATION

The five-transistor implication cell can be reduced to a three-transistor cell by removing the *true* reference current-mirror buffers (Figure 10, shaded). The reference currents are already generated by an array of current mirrors elsewhere on the ŁLA. This current-mirror array must be implemented with pMOS current mirrors to provide current-source outputs instead of current sinks.



(a) Current source cell (b) Current sink cell (c) Three-transistor implication pair

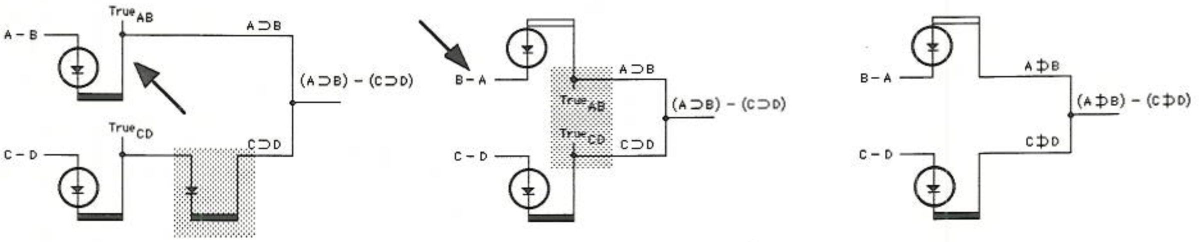
Figure 10. Removing *true* reference current mirrors.

The *true* reference currents can be used to adjust the output value of the paired implication cell. The reference current-mirror array is separated into one array of *true* references for the current-source cells and another array for the current-sink cells. Each array is driven by a separate external input. Adjusting these inputs with respect to each other changes the location of the minimal error in each quadrant of the circuit's output. This adjustment can be used to compute functions with improved accuracy, although the precision of the circuit is unchanged.

2.1.4 ONE-DIODE NEGATED IMPLICATION

The implication cell can be reduced to a single diode by transforming it to negated implication. In this process two-transistor and one-transistor negated implication cells are described. All active elements of the implication pair except the diode-connected MOSFET are removed, which is replaced by one diode.

The first step in the transformation is to remove the current sink in the current-sink cell (Figure 11a, shaded). Next, the sign of the *true* reference current is changed. To accomplish this the current-source cell is "inverted" by changing the nMOS current mirror to a pMOS current mirror, and the *true* reference current to a current sink (Figures 11a and 11b). The sign of the α and β inputs must be reversed to preserve the computation of *min(true, true –* $\alpha + \beta$*)* (Figure 11b, arrow). The *true* reference currents are removed because their signs are opposite; they subtract out according to Kirchoff's Law (Figure 11b, shaded). A pair of two-transistor negated implication cells remain (Figure 12c). Each cell computes *max(0,* $\alpha - \beta$*)*.



(a) (b) (c)

Figure 11. Inverting current source cell polarity to eliminate reference currents.

The simplified schematic is expanded to show the derivation of the one-diode implication circuit (Figure 12a is equivalent to Figure 12b). The transistors that implement the current source and current sink outputs (Figure 12b, shaded) are not needed if the output voltage is sufficient to forward-bias the next diode-connected MOSFET in the array. (If not, the voltage can be restored by inserting a buffer.) Thus each current mirror can be replaced by a diode-connected MOSFET (Figure 12c). Substituting a p-n junction diode or a Schottky diode for the diode-connected MOSFET yields the one-diode implication cell (Figure 12d).

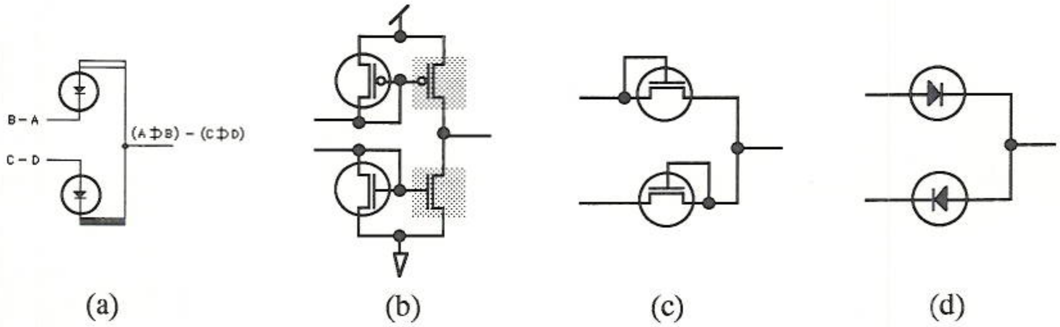


Figure 12. Reducing current mirrors to diodes.

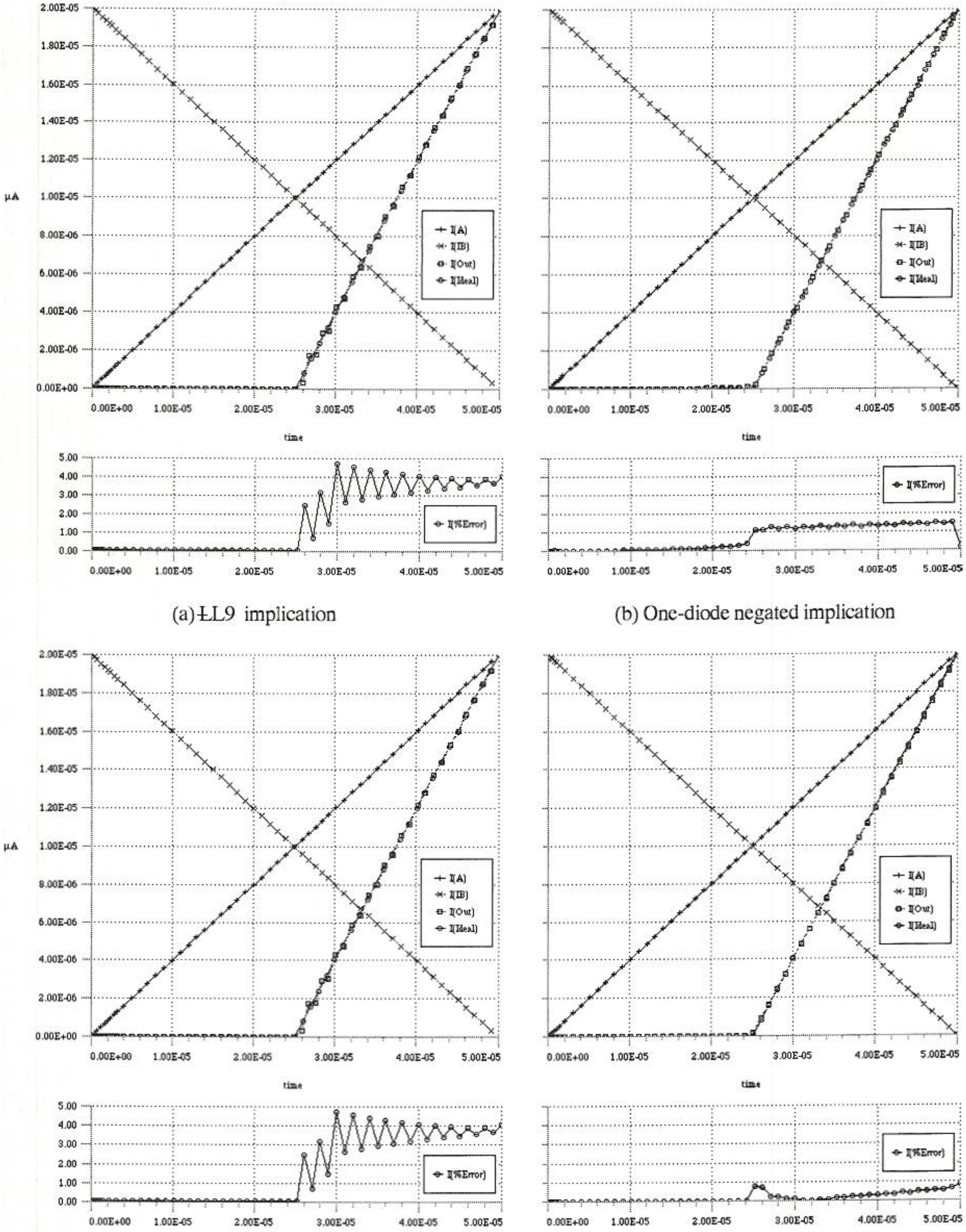
Analog computers of the 1950's and 1960's used diodes to build special function generators [12, 13]. However, the link between these special function generators and Łukasiewicz logic was not recognized, although Wilkinson described an "analog diode logic" that is equivalent to Łukasiewicz logic [14]. Mead's innovations in analog VLSI for neural systems [15], the use of Łukasiewicz logic as a foundation for approximate reasoning systems, and the advent of practical ŁLAs point to the renewed growth of analog computing after a 30-year hiatus.

2.2 EVALUATING THE THREE-TRANSISTOR AND ONE-DIODE IMPLICATION CIRCUITS

The results of simulating the ŁL9, the three-transistor, and the one-diode implication cells are shown. Level 3 of Spice is used because it most closely matches the measurements obtained from ŁL9. All simulations use the MOSIS process parameters for the ŁL9 fabrication run.

The "half-notch" function is simulated. It is defined by the expression $\neg\ (\ \alpha \supset \neg\ \alpha\ )$. The maximum error of the ŁL9 simulation is near 5% (Figure 13a and 13c), which is greater than the 4% error of an untrimmed ŁL9. The one-diode implication cell has a maximum error of 1.5% (Figure 13b). The three-transistor implication cell has a maximum error of 0.8% (Figure 13d). The smaller error in the one-diode implication cell is probably due to fewer active components, which reduce the noise in the cell's output. The three-transistor cell uses the *true* reference inputs to trim the cell's output. Varying the trim inputs is equivalent to varying the gain ratio between the current-source and current-sink implication cells in each pair, which reduces the error in the output.

Measurements of ŁL9 show that its typical error is less than 2%, with a mean error less than 0.5% [1, 4]. This suggests that the results of simulating the three-transistor and the one-diode implication cells are plausible.



(a) ŁL9 implication

(b) One-diode negated implication

(c) ŁL9 implication

(d) Three-transistor implication

Figure 13. Comparing simulations of implication cells.

3. VERY DENSE ŁLAS

Two new ŁLAs are proposed in this paper. The first is a trimmable ŁLA based on the three-transistor implication cell. It is referred to as the three-transistor ŁLA and is similar to the prototype ŁLA. The second is a very dense ŁLA based on one-diode negated implication. The negated implication circuits are implemented in pairs, using two Schottky diodes stacked vertically. This three-dimensional VLSI structure is called a *diode tower*, so the ŁLA incorporating it is referred to as a diode-tower ŁLA.

3.1 THREE-TRANSISTOR ŁLAS

The three-transistor ŁLA is smaller than ŁL9 because it contains fewer transistors, and because those transistors are the same type. Because only nMOS transistors are used, no area is wasted to separate p-wells and n-wells internally. The pMOS current mirrors in the leaf input cells and the *true* reference current mirror array are placed around the edge of the ŁLA. The nMOS current mirrors are grouped in the interior and root nodes (Figure 14a). The electrical isolation and heat dissipation of the ŁLA is improved by covering the pMOS devices with a metal2 V_{dd} plane; the nMOS devices are covered with a metal2 GND plane (Figure 14b).

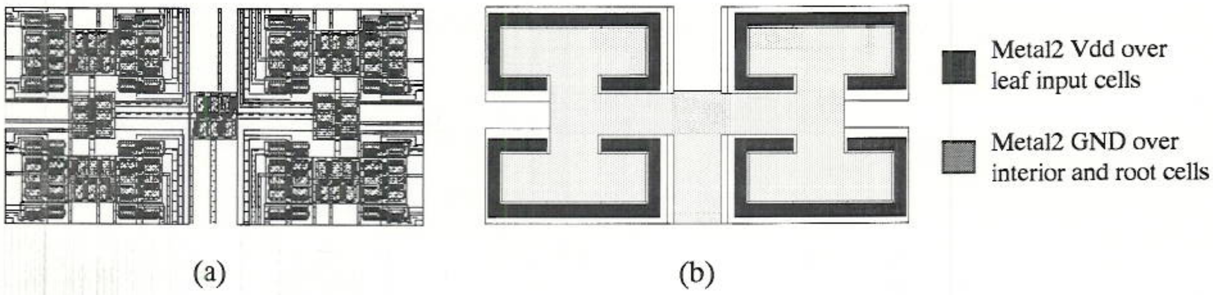

Metal2 Vdd over leaf input cells
Metal2 GND over interior and root cells
(a)
(b)

Figure 14. Layout of 31-cell ŁLP-3FET array.

3.2 DIODE TOWER ŁLAS

A three-dimensional VLSI structure, the *diode tower*, is proposed to implement very dense ŁLAs. A diode tower is a vertically-oriented one-diode implication pair embedded in a silicon dioxide matrix. Diode towers can be constructed from p-n or Schottky diodes. P-n diode towers can be fabricated using three-dimensional silicon-on-insulator process technology, which has already been developed for MOSFETs. P-n diode towers are prevented from becoming avalanche diodes [16] by the central output connection of the diode tower. Diode towers can also be fabricated using bulk CMOS processes by intentionally building Schottky diodes, the normally unwanted devices that result when metal directly contacts diffusion.

In the proposed Schottky diode tower, the metal-diffusion contacts are not disabled by a layer of heavily-implanted n+ diffusion, except where an ohmic connection is desired between the diodes in the diode tower (Figure 15). The integral metal layers in the Schottky diodes are extended as global routing planes. N+ diffusion locally connects buried contacts in the substrate (Figure 16a).

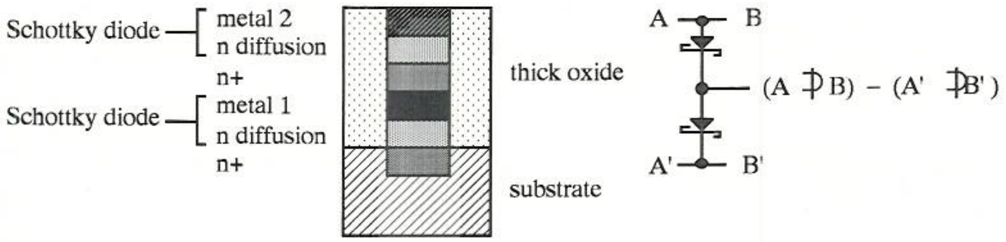


Figure 15. Diode tower.

Using diode towers standard-cell ŁLAs can be designed as a *sea of implications.* These devices bring contacts for connections between cells to the surface of the ŁLA and leave them open for routing at a later time (Figure 16a). One diode-tower (two implication cells) can be constructed within a $6\times10\lambda^2$ area (Figure 16c) and tiled as shown to give four diode towers (eight implications) per $14\lambda^2$ (Figure 16b). In this configuration a 2μ process would fit a maximum of 36,000 implications into a MOSIS Tiny Chip, and approximately 1.3×10^6 implications into a one cm^2 die. This is the equivalent of 10^4 fuzzy rules or algebraic functions.

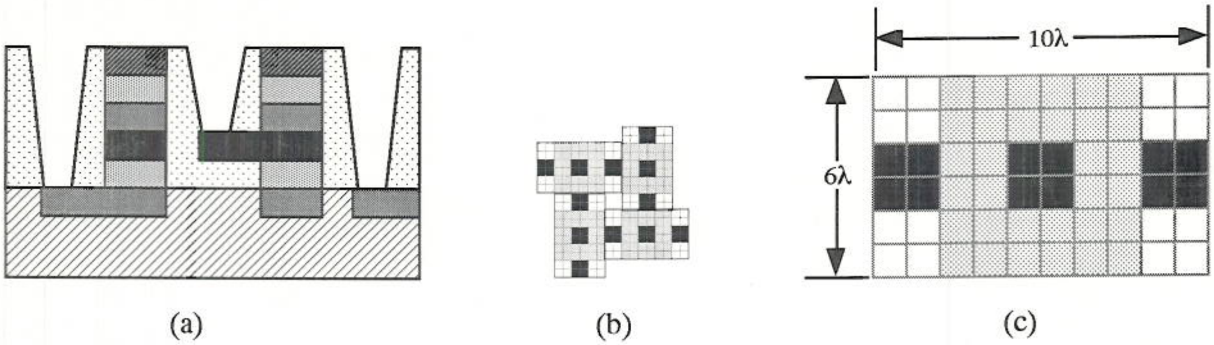
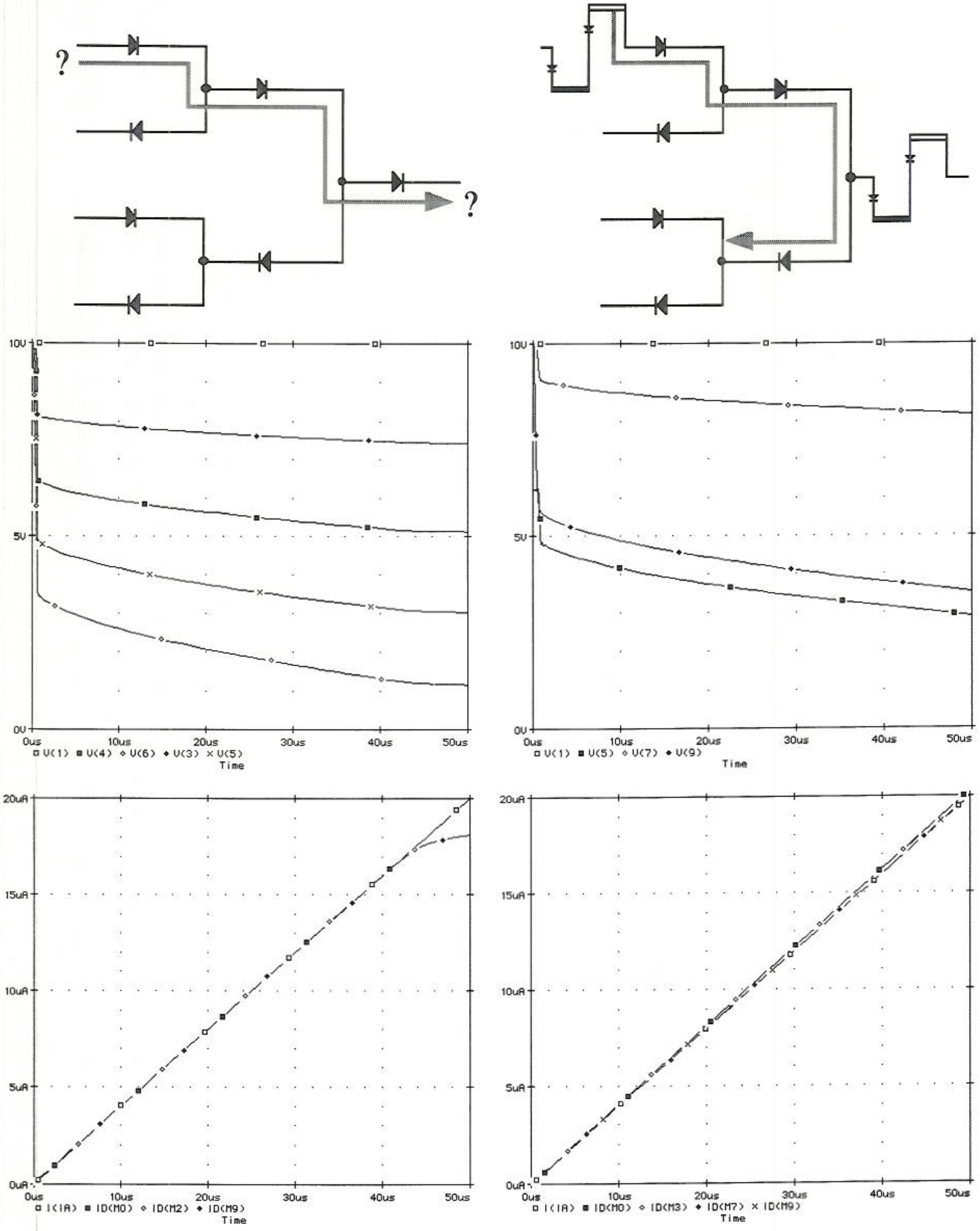


Figure 16. Diode tower array.

The one-diode negated implication circuit has the disadvantage that the voltage drop across successive diodes in a chain will be insufficient to forward-bias the last diode in the chain (Figure 17a). Current-mirror buffers, similar to buffers in digital logic, must be inserted to prevent this from occurring (Figure 17b). A buffer is needed after every three diode-connected MOSFETs, which have a voltage drop of 1.2 volts, or every 10 to 15 Schottky diodes, which have a voltage drop of 0.25 volts.



(a) Without buffer

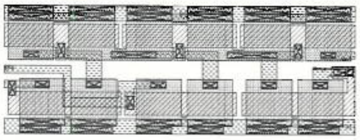
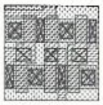
(b) With buffer

Figure 17. Unbuffered and buffered one-diode negated implication chains in an ŁLA.

3.3 ADVANTAGES AND DISADVANTAGES OF VERY DENSE ŁLAS

Diode-tower and three-transistor ŁLAs are denser than previous designs. In an 1800μ × 2000μ area the diode-tower ŁLA contains 36,000 implications, while the three-transistor ŁLA contains 1,990 implications. Only 92 12-transistor implications fit into the same area. Table 1 summarizes the improvements.

Table 1. Optimization of ŁLAs.

ŁLA	Cell layout (all to same scale) Cell type, number of components	Function	Area of 31 cell array[2]	Maximum implications	
				"Tiny" chip	1 cm^2 area
ŁL9	 stand-alone MOSFET, 6 pTrans + 6 nTrans	$\alpha \supset \beta$	888μ x 1366μ	92	2,550
ŁLA-3FET	 Cascoded MOSFET, 3 nTrans	$\alpha \supset \beta$	170μ x 329μ	1,990	55,400
ŁLA-D-3d (proposed)	Cascoded diode tower, 1 Schottky diode	$\alpha \not\supset \beta$	48μ x 48μ	36,000	1,300,000

A disadvantage of diode-tower ŁLAs is that the voltage drop across successive diodes in a chain will be insufficient to forward-bias the last diode in the chain. Circuits similar to buffers in digital logic must be inserted to prevent this from occurring.

An advantage of three-transistor ŁLAs is that they can be fabricated using nMOS current mirrors alone. The resulting array is less dense than the diode tower array, but functions more accurately. The trim inputs can be adjusted to reduce error to less than 1% of full scale. This ŁLA is more accurate than the prototype ŁL9 because its output can be trimmed using independent positive and negative reference currents.

Both ŁLAs have the advantage that the number of inputs is twice the number of input pins on the package. This is because each input is the difference of two currents, which can be computed externally and carried on a single wire.

[2] Values measured from MAGIC layouts for MOSIS 2μ SCPE Orbit process, or estimated for 2μ 3-D process.

4. SUMMARY AND CURRENT WORK

A one-diode circuit for negated implication ($\not\supset$) and an adjustable three-transistor implication circuit with maximum error less than 1% of full scale were described. Two ŁLAs were proposed that use area-efficient implementations of the one-diode and three-transistor implication circuits. The very dense diode-tower ŁLA contains 36,000 implications in an area that previously held 92 implications; the three-transistor ŁLA contains 1,990 implications. Both ŁLAs double the number of inputs per pin on the IC package.

Diode tower designs for very-dense three-dimensional ŁLAs are now being simulated. If these designs are successful, then the next generation of ŁLAs may fit as many as 1.3 million implications into a one cm^2 area. Very dense ŁLAs are needed to make ŁLA-based architectures for neural networks and fuzzy controllers practical.

ŁLA simulators are being applied to neural networks and fuzzy controllers. The Sharks & Jets constraint propagation network has been simulated with ŁLAs [17]. A simple fuzzy controller for an air conditioner has been designed that uses three implications to implement a continuously-varying number of rules. This fuzzy controller fits into a $100\mu^2$ area.

Achernar, believed to be the first analog compiler since the 1970's, is being developed by Andy Heininger, a graduate student in the Analog VLSI Laboratory. Achernar compiles algebraic expressions to Łukasiewicz implication, uses tree-pattern matching to minimize the tree, and applies peephole optimizations to further simplify the expression. The output of Achernar is a sentence schema for an ŁLA from which a MAGIC layout of a very dense ŁLA can be extracted.

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