Geoffrey M. Brown

Professor of Computer Science

School of Informatics and Computing
Lindley Hall 330
Indiana University
Bloomington, IN 47405

812 855-4207
geobrown@indiana.edu

Prepared December 6, 2017

Employment

2013 – 2014	Program Manager, National Science Foundation, CISE/CNS
2007 – Present	Tenured Professor of Computer Science, Indiana University
2007 – 2010	CS Director of Undergraduate Studies, Indiana University
2003 – 2007	Tenured Associate Professor of Computer Science, Indiana University
8/2001 – 2003	Chief Architect, Sockeye Networks
2/2001 – 7/2001	Architect, Turin Networks
2000 – 2/2001	Software Architect, IronBridge Networks
1997 – 2000	Research Scientist, Hewlett Packard Laboratories. HP Co-lead for design of the HP/ST LX/ST2xx family of VLIW microprocessors.
1987 – 1997	Assistant, Associate Professor with Tenure (fall 1993), Cornell University School of Electrical Engineering and graduate field of Computer Science
1983 – 1984	Engineer, Motorola Semiconductor

Education

1987 PhD, Electrical Engineering, The University of Texas at Austin (Dissertation: Self-Stabilizing Distributed Resource Allocation)

1983 MS, Electrical Engineering, Stanford University

1982 BS, Engineering, Swarthmore College

Honors

2006 School of Informatics Trustees Teaching Award

1993 SERC Visiting Fellow Oxford University

1990 NSF Presidential Young Investigator Award

1987 DuPont Fellowship University of Texas

1983 – 1986 Microelectronics and Computer Development Fellowship University of Texas

1983 General Electric Foundation Fellowship Stanford University

Courses Taught

Numbers in parenthesis represent students/section.

Indiana University

H|C335 Computer Structures Spring 2005 (10), Fall 2005 (24), Fall 2006 (25), Fall 2007, (26), Fall 2008 (25), Fall 2009 (36), Fall 2010 (32), Fall 2011 (35), Fall 2012 (26), Spring 2015 (47), Fall 2015 (20), Spring 2016 (56),

P436 Operating Systems Fall 2003 (35), Fall 2004 (36), Fall 2005 (30), Fall 2006 (25)

B441/541 Digital Design Spring 2008 (15), Spring 2009 (12)

B524 Parallel Computing Spring 2015 (10).

B649 Digital Preservation Spring 2007 (12), Fall 2007 (8), Spring 2010 (10), Fall 2011 (12)

B649 Concurrent Languages For System Design Spring 2003 (10)

Cornell University

EE230 Introduction to Digital Systems Spring 1994 (80), Spring 1995 (45), Fall 1995 (150), Spring 1996 (40)

EE475 Computer Structures, Fall 1990 (65), Fall 1991 (94), Fall 1992 (70), 1994 (80).

EE545 Computer Networks, Fall 1987 (70), 1988 (85) , 1989 (55)

EE546 Computer Networks II, Spring 1993 (40)

EE591 Compiling Concurrent Languages for Field Programmable Gate Arrays, Fall 1996 (3).

EE594 Introduction to Protocol Design, Spring 1992 (19).

EE594 Formal Methods for Hardware Design, Spring 1988 (12), 1989 (15), 1990 (12)

CS711 Process Algebras, Fall 1990 (13).

Professional Activities

Advisory Group Bitcurator project (`www.bitcurator.net`) 2011–2012, 2014–2016.

Program Committee *IEEE 20th International Conference on Application-Specific Systems, Architectures and Processors*, 2009.

Program Committee *SAMOS IX: International Symposium on Systems Architectures Modeling and Simulation*, 2009

Program Committee *IEEE 19th International Conference on Application-Specific Systems, Architectures and Processors*, 2008.

Program Chair *IEEE 17th International Conference on Application-specific Systems, Architectures and Processors*

Program Committee *IEEE 17th International Conference on Application-Specific Architectures and Processors*, 2006. DOI 10.1109/ASAP.2006.55

Program Committee *SAMOS VI: Embedded Computer Systems: Architectures, Modeling, and Simulation*, 2006

Visiting Faculty *TU Delft*, 2006

Program Committee *Third ACM-IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE'2005)*, 2005

Program Committee *DATE – Design, Automation and Test in Europe*, 2005.

Program Committee *IEEE International Conference on Field-Programmable Technology*, 2004

Program Committee *IEEE International Conference on Field-Programmable Technology*, 2003

Program Committee *MICRO-34 IEEE/ACM International Symposium on Microarchitecture*, 2001.

Swarthmore College Engineering Council 1996-2001.

Visiting Faculty Intel, July 1992.

Program Committee *SIGCOMM 89 Communications Architectures and Protocols*

Session-chair *SIGCOMM 89 Communications Architectures and Protocols*

Chair-person *MSI Workshop on Hardware Specification, Verification, and Synthesis: Mathematical Aspects*, Ithaca, NY, July 1989

Treasurer IEEE, Ithaca Branch, 1988-1989

Consulting AT&T Bell Laboratories (Summer 1988, May 1991), Codenol (December 1990).

Department and University Service

Engineering BS Committee 2015.

Chair of CS Colloquium Committee 2015–2016.

Chair of CS Faculty Recruiting Committee 2010-2011.

Bloomington Faculty Council 2010.

Bloomington Budgetary Affairs Committee Fall 2010.

Search Committee for Vice-Provost for Undergraduate Education 2008.

Co-chair Informatics Undergraduate Strategic Planning Committee 2007.

CS Director of Undergraduate Studies 2007-2010.

University General Education Committee 2006-2007.

CS Systems Qualifying Exam 2003-2004.

CS Undergraduate Education Committee 2004–2010, 2012, 2015

CS Faculty Affairs Committee 2005, 2007.

CS Admission and Awards Committee 2003.

CS Hiring Committee (Embedded Systems) 2003.

EE Policy Committee 1991 – 1996.

Faculty Council of Representatives 1991 – 1994.

EE Computer Engineering Recruiting Committee 1992.

EE Student/Faculty Committee 1990-1991.

EE Curriculum and Standards Committee 1988-1990.

EE Opto Electronics Recruiting Committee 1989-1990.

EE Information Technology Recruiting Committee 1994 – 1996.

EE Computer Policy Committee 1988-1989.

Research Support

Note: I had to relinquish my active grants when I served as an NSF program officer 2012-2014.

Active Support:

2016 – 2018	EAGER: Novel Ultralight Sensors for Avian Migration and Movement Studies NSF 1644717 Role: Principal Investigator Amount:$298,069
2015–2017	EAGER: Portable, Secure Emulation for Digital Preservation NSF 1529415 Role: Principal Investigator Amount: $205,563

Past support:

2011–2012	Reversible Concurrency NSF 1116725 Role: Co-investigator (PI Amr Sabry) Amount: $317,477
2010–2012	Assisted Emulation for Digital Preservation NSF 1016967 Role: Principal Investigator Amount: $181,969
2010-2011	Enabling High-Quality Format Migration of Scientific Data D2I Center Indiana University Role: Principal Investigator Amount $47,992
1996–1997	Data Acquisition Systems with User Configurable Hardware NSF 9530811 Role: Principal Investigator Amount: $162,295
1993–1996	Joint Research in Hardware Synthesis and Verification NSF 9224575 Role: Principal Investigator Amount: $20,000
1990–1997	Presidential Young Investigator Award: Formal Verification of Hardware Synthesis Systems

	NSF 9058180 Role: Principal Investigator Amount: $322,406
1992	Special Purpose Grant for Researching Communication Protocols AT&T Role: Principal Investigator Amount: $10,000
1992	Visiting Faculty Intel Role: Principal Investigator Amount: $10,000
1990–1996	PYI Matching Funds AT&T Role: Principal Investigator Amount: $75,000
1990	Research Initiation Grant Awarded, but withdrawn due to PYI NSF Role: Principal Investigator
1991	HP9000/720 Computer Hewlett Packard Role: Principal Investigator Amount: $24,000
1989	Mobil Scholar Award Mobil Corporation Role: Principal Investigator Amount: $10,000
1988	Protocols and Broadband Integrated Digital Networks AT&T Role: Principal Investigator Amount: $30,000

Teaching Support

Funding I raised to support laboratory courses I was developing.

2010–2015	Components for C335 ST Microelectronics Amount: $5000
2007	Components and Software for B441 Altera Amount $1000
2006	Components for C335 Philips Semiconductor Amount: $500
2004	Components for C335 Texas Instruments Amount: $1100
2004	Goofy Giggles Toys for C335 Little Tikes Amount: $750
1995	Computer Upgrades for EE Labs Intel Amount: $106,145
1995	Digital Project Lab Intel Amount: $44,500
1995	Digital Design Lab Development Intel Amount: $5,823
1994	PLD Development Software Altera Amount: $45,500
1994	Computer for Course Development Intel Amount: $7,614
1994	Computer for System Staff Intel

Amount: $9,432

1994 Computers for EE Undergraduate Lab
Intel
Amount: $167,238

1993 Computers for Digital Lab
Intel
Amount: $38,346

1993 Logic Analyzers
Hewlett-Packard
Amount: $30,577

1992 PLD Development Software & Hardware
Altera
Amount: $145,925

1992 Protoboard Fabrication for EE475
Intel
Amount: $2963

1992 Computers for EE Undergraduate Lab
Intel
Amount: $83,484

1992 Protoboard Fabrication for EE230
Intel
Amount: $18,111

1991 Components and Programmers
AMD
Amount: $4000

1991 Software and Hardware for EE475
Intel
Amount: $92,022

1991 Software and I/O boards
National Instruments
Amount: $4500

1991 Undergraduate Research
Moore Fund (Cornell)
Amount: $900

1988 Micromouse Team
Moore Fund (Cornell)
Amount: $2400

Publications

Publication gaps reflect time as program director at NSF and in industry where work developed was proprietary (see patent listings). Since my return to IU from NSF, I have developed and received federal funding for two new projects.

Patents

[1] Fred Homewood, Gary Vondran, Geoffrey Brown, and Paolo Faraboschi. System and method for reducing power consumption in a data processor having a clustered architecture, August 2010. US 7,779,240.

[2] Fred Homewood, Gary Vondran, Geoffrey Brown, and Paolo Faraboschi. Executing conditional branch instructions in a data processor having a clustered architecture, 2008. US 7,337,306.

[3] Paolo Faraboschi, Anthony Jarvis, Fred Homewood, Geoffrey Brown, and Gary Vondran. Circuit and method for instruction compression and dispersal in wide-issue processors, 2006. US 7,143,268.

[4] Fred Homewood, Anthony Jarvis, Alex Starr, Geoffrey Brown, Paolo Faraboschi, and Gary Vondran. System and method for encoding constant operands in a wide issue processor, 2005. US 6,922,733.

[5] Paolo Faraboschi, Alexander Starr, Geoffrey Brown, and Mark Own Homewood. Circuit and method for supporting misaligned accesses in the presence of speculative load instructions, 2004. US 6,829,700.

[6] Paolo Faraboschi, Alexander Starr, Geoffrey Brown, and Richard Ford. Circuit and method for hardware-assisted software flushing of data and instruction caches, 2004. US 6,691,210.

Patents Applied For

[7] Geoffrey Brown. Network address space clustering employing topological groupings, distance measurements, and structural generalization, 2004. 20040059830.

Book

[8] Geoffrey Brown. *Discovering the STM32 Microcontroller*. Released under Creative Commons License, 2012.

Edited Book

[9] Miriam Leeser and Geoffrey Brown, editors. *Hardware Specification, Verification and Synthesis: Mathematical Aspects, Mathematical Science Institute Workshop, Cornell University, Ithaca, New York, USA, July 5-7, 1989, Proceedings*, volume 408 of *Lecture Notes in Computer Science*. Springer, 1990.

Peer Reviewed Papers

[10] Geoffrey Brown. Developing virtual cd-rom collections: The voyager company publications. *International Journal of Digital Curation*, 7(2), 2012.

[11] Chris Frisz, Geoffrey Brown, and Samuel Waggoner. Assessing migration risk for scientific data formats. *International Journal of Digital Curation*, 7(1), 2012.

[12] Aaron Hsu and Geoffrey Brown. Dependency analysis of legacy digital materials to support emulation based preservation. *International Journal of Digital Curation*, 6(1), 2011.

[13] Kam Woods and Geoffrey Brown. Born broken: Fonts and information loss in legacy digital documents. *International Journal of Digital Curation*, 5(1), 2011.

[14] Kam Woods and Geoffrey Brown. Assisted emulation for legacy executables. *International Journal of Digital Curation*, 5(1), 2010.

[15] Bhanu Pisupati and Geoffrey Brown. Embedded software debugging using virtual file system abstractions. *Journal of Systems Architecture*, (56):487–499, 2010.

[16] Geoffrey M. Brown and Lee Pike. Automated verification and refinement for physical-layer protocols. *Formal Aspects of Computing*, 23(3):243–266, 2010. DOI:10.1007/s00165-010-0149-0.

[17] Kam Woods and Geoffrey Brown. Creating virtual cd-rom collections. *International Journal of Digital Curation*, 4(2), 2009.

[18] Kam Woods and Geoffrey Brown. Migration performance for legacy data access. *International Journal of Digital Curation*, 3(2), 2008.

[19] S. Yusef, W. Luk, M. Sloman, N. Dulay, E.C. Lyon, and G. Brown. Reconfigurable architecture for network flow analysis. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 16(1):57–65, January 2008.

[20] John O'Leary, Geoffrey Brown, and Wayne Luk. Verified compilation of communicating processes into clocked circuits. *Formal Aspects of Computing*, 9(5-6):537–559, 1997.

[21] John O'Leary and Geoffrey Brown. Synchronous emulation of asynchronous circuits. *IEEE Transactions on Computer Aided Design of Integrated Circuits*, 16(12):1514–1521, 1997.

[22] Geoffrey Brown, Wayne Luk, and John O'Leary. Retargeting a hardware compiler using protocol converters. *Formal Aspects of Computing*, 8(2):209–237, 1996.

[23] Geoffrey Brown and Norman Vrana. A computer architecture laboratory course using programmable logic. *IEEE Transactions on Education*, 38(2):118–125, May 1995.

[24] Alan S. Wenban, John O'Leary, and Geoffrey Brown. Codesign of communication protocols. *IEEE Computer*, 26(12):46–52, 1993.

[25] Yehuda Afek and Geoffrey Brown. Self-stabilization over unreliable communication media. *Distributed Computing*, 7(1):27–34, 1993.

[26] Yehuda Afek, Geoffrey Brown, and Michael Merritt. Lazy caching. *ACM Transactions on Programming Languages and Systems*, 15(1):182–205, 1993. This paper was the subject of a special issue of *Distributed Computing,* 12(2/3), 1999.

[27] David Basin, Geoffrey Brown, and Miriam Leeser. Formally verified synthesis of combinational cmos circuits. *Integration VLSI Journal*, 11(3):235–250, 1991.

[28] Geoffrey Brown, Mohamed Gouda, and Raymond Miller. Block acknowledgments, redesigning the window protocol. *IEEE Transactions on Communications*, 39(4):524–532, April 1991.

[29] Wayne Luk and Geoffrey Brown. A systolic lru processor and its top-down development. *Science of Computer Programming*, 15(2-3):217–233, 1990.

[30] Geoffrey Brown. Asynchronous multicaches. *Distributed Computing*, 4(1):31–36, 1990.

[31] Geoffrey Brown, Mohamed Gouda, and Chuan-Lin Wu. Token systems that self-stabilize. *IEEE Transactions on Computers*, 38(6):845–852, 1989.

Reviewed Conference Papers

[32] Zahra Tarkhani, Geoffrey Brown, and Steven Myers. Trustworthy and portable emulation platform for digital preservation. In *14th International Conference on Preservation of Digital Objects (iPRES)*, 2017.

[33] Geoffrey Brown and Amr Sabry. Reversible communicating processes. In *Workshop on Programming Language Approaches to Concurrency and Communication. PLACES 2015*, 2015.

[34] Omer Arap, Geoffrey Brown Martin Swany, and Bryce Himebaugh. Adaptive recursive doubling algorithms for collective communication. In *Parallel & Distributed Processing Symposium Workshops (IPDPSW)*, May 2015.

[35] Omer Arap, Geoffrey Brown, Bryce Himebaugh, and Martin Swany. Software defined multicasting for MPI collective operation with offloading with the NetFPGA. In *Euro-Par 2014*, pages 632–643, 2014.

[36] Omer Arap, Geoffrey Brown, Bryce Himebaugh, and Martin Swany. Implementing MPI barrier with the NetFPGA,offloading with the netfpga. In *20th International Conference on Parallel and Distributed Processing Techniques and Applications*, 2014.

[37] Swetha Toshniwal, Geoffrey Brown, Kevin Cornelius, Gavin Whelan, and Enrique Areyan. Evaluating assisted emulation for legacy executables. In *9th International Conference on Preservation of Digital Objects (iPRES)*, 2012.

[38] Geoffrey Brown. Developing virtual cd-rom collections: The voyager company publications. In *8th International Conference on Preservation of Digital Objects (iPRES)*, 2011.

[39] Chris Frisz and Geoffrey Brown. Assessing migration risks for scientific data. In *7th International Digital Curation Conference*, 2011.

[40] Aaron Hsu and Geoffrey Brown. Dependency analysis of legacy digital materials to support emulation based preservation. In *6th International Digital Curation Conference*, 2010.

[41] Bhanu Pisupati and Geoffrey Brown. Configuration & deployment of sensor network applications using file system abstractions. In *First International Workshop on Advances in Wireless Sensor and Actuator Networks – AWSAN 10*, 2010.

[42] Kam Woods and Geoffrey Brown. Assisted emulation for legacy executables. In *5th International Digital Curation Conference*, 2009.

[43] Geoffrey Brown and Kam Woods. Born broken:fonts and information loss in legacy digital documents. In *The Sixth International Conference on Preservation of Digital Objects iPRES*, October 2009.

[44] Lee Pike, Geoffrey Brown, and Alwyn Goodloe. Roll your own test bed for embedded real-time protocols: A haskell experience. In *Haskell Symposium*, page to appear, September 2009.

[45] Kam Woods and Geoffrey Brown. From imaging to access: Effective preservation of legacy removable media. In *Archiving 2009*, pages 213–218, May 2009.

[46] Kam Woods and Geoffrey Brown. Creating virtual cd-rom collection. In *iPRES 2008: The Fifth International Conference on Preservation of Digital Objects*, 2008.

[47] Stephan Wong, Thijs van As, and Geoffrey Brown. ρ-vex: A reconfigurable and extensible softcore vliw processor (poster session). In *International Conference on Field-Programmable Technology*, 2008.

[48] Markus Koester, Wayne Luk, and Geoffrey Brown. A hardware compilation flow for instance-specific vliw cores (poster session). In *International Conference on Field Programmable Logic and Applications*, 2008.

[49] Kam Woods and Geoffrey Brown. Migration performance for legacy data access. In *3rd Digital Curation Conference*, 2007.

[50] Thomas Reichherzer and Geoffrey Brown. Quantifying software requirements for supporting archived office documents using emulation. In *Joint Conference on Digital Libraries (JCDL)*, 2006.

[51] Geoffrey Brown and Lee Pike. Temporal refinement using smt and model checking with an application to physical-layer protocols. In *Proceedings of Formal Methods and Models for Codesign (MEMOCODE'2007)*, pages 171–180. OmniPress, 2007. Available at `http://www.cs.indiana.edu/~lepike/pub_pages/refinement.html`.

[52] Geoffrey Brown. Verification of a data synchronization circuit for all time. In *6th International Conference on Application of Concurrency to System Design (ACSD)*, 2006.

[53] Bhanu Pisupati and Geoffrey Brown. File system framework for organizing sensor networks (poster session). In *26th ACM Symposium on Applied Computing*, 2006.

[54] Geoffrey Brown and Lee Pike. Easy parameterized verification of biphase mark and 8n1 decoders. In *International Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS)*, volume 3920 of *Lecture Notes in Computer Science*, pages 58–72, 2006.

[55] Bhanu Pisupati and Geoffrey Brown. File system interfaces for embedded software development. In *23rd International Conference on Computer Design (ICCD 2005)*, pages 232–238, 2005.

[56] Sameer Tilak, Bhanu Pisupati, Kenneth Chiu, Geoffrey Brown, and Nael Abu-Ghazaleh. A file system abstraction for sense and respond systems. In *EESR '05: Proceedings of the 2005 workshop on End-to-end, sense-and-respond systems, applications and services*, pages 1–6, Berkeley, CA, USA, 2005. USENIX Association.

[57] Wayne Luk, Sherif Yusuf, Morris Sloman, Geoffrey Brown, Emil C. Lupu, and Naranker Dulay. A combined hardware-software architecture for network flow. In *Proceedings of The 2005 International Conference on Engineering of Reconfigurable Systems and Algorithms, ERSA 2005*, pages 149–155, 2005.

[58] Paolo Faraboschi, Geoffrey Brown, Joseph A. Fisher, Giuseppe Desoli, and Fred Homewood. Lx: a technology platform for customizable VLIW embedded processing. In *Proceedings of International Symposium of Computer Architecture (ISCA)*, pages 203–213, 2000.

[59] Jifeng He, Geoffrey Brown, Wayne Luk, and John W. O'Leary. Deriving handshake modules for a multi-target hardware compiler. In *Designing Correct Circuits*. Springer Electronic Workshop in Computer Series, 1996.

[60] Geoffrey Brown. User-configurable data acquisition systems. In John Schewel, Peter Athanas, V. Michael Bove, and John Watson, editors, *Proceedings High-Speed Computing, Digital Signal Processing, and Filtering Using Reconfigurable Logic*, volume 2914, pages 54–64. SPIE, 1996.

[61] Alan Wenban and Geoffrey Brown. A software development system for fpga-based data acquisition systems. In *IEEE Symposium on FPGAs for Custom Computing Machines*, pages 28–37, 1996.

[62] Alan S. Wenban, Geoffrey Brown, and John O'Leary. Developing interface libraries for reconfigurable data acquisition boards. In *FPL '95: Proceedings of the 5th International Workshop on Field-Programmable Logic and Applications*, volume 975 of *Lecture Notes in Computer Science (LNCS)*, pages 331–340, London, UK, 1995. Springer-Verlag.

[63] Geoffrey Brown, Wayne Luk, and John O'Leary. Retargeting a hardware compiler proof using protocol converters. In *International Symposium on Advanced Research in Asynchronous Circuits*, pages 54–63. IEEE, 1994.

[64] Alan Wenban, John O'Leary, and Geoffrey Brown. Codesign of communication protocols. In *International Workshop on Software/Hardware Codesign*, 1992.

[65] Sam Weber, Bard Bloom, and Geoffrey Brown. Compiling joy into silicon: An exercise in applied structural operational semantics. In *Semantics: Foundations and Applications, REX Workshop*, volume 666 of *Lecture Notes in Computer Science*, pages 639–659, 1992.

[66] Sam Weber, Bard Bloom, and Geoffrey Brown. Compiling joy into silicon. In Thomas Knight and John Savage, editors, *Brown/MIT Conference on Advanced Research in VLSI and Parallel Systems*, pages 79–98, 1992.

[67] Richard Chapman, Geoffrey Brown, and Miriam Lesser. Verified high-level synthesis in BEDROC. In *European Design Automation Conference*, pages 59–63. IEEE, 1992.

[68] Chee-Keng Chang, Geoffrey Brown, and Miriam Lesser. "EDISYN: A Language-Based Editor for High-Level Synthesis". In D. Borrione and R. Waxman, editors, *CHDL 91 - Computer Hardware Description Languages and their Application*, pages 339–357, Marseille, France, April 1991. North-Holland.

[69] Geoffrey Brown and Michael Merritt. Hierarchical lazy caches. In *28th Allerton Conference on Communication, Control, and Computing*, pages 548–557, October 1990.

[70] Geoffrey Brown. Towards truly delay insensitive circuit realizations of process algebras. In *Workshop on Designing Correct Circuits*, Workshops in Computer Science, pages 120–131. Springer-Verlag, September 1990.

[71] David Basin, Geoffrey Brown, and Miriam Leeser. Formally verified synthesis of cmos. In *IMEC-IFIP International Workshop on: Applied Formal Methods For Correct VLSI Design*, volume 1, pages 197–208, Leuven, Belgium, 1989.

[72] Yehuda Afek and Geoffrey Brown. Self-stabilization of the alternating-bit protocol. In *Eighth IEEE Symposium on Reliable Distributed Systems*, pages 80–83, 1989.

[73] Miriam Leeser and Geoffrey Brown. Verifying high-level hardware synthesis tools. In *Fourth International Workshop on High-Level Synthesis*, October 1989.

[74] Geoffrey Brown, Mohamed Gouda, and Raymond Miller. Block acknowledgment: redesigning the window protocol. In *SIGCOMM '89: Symposium proceedings on Communications architectures & protocols*, pages 128–135, New York, NY, USA, 1989. ACM Press.

[75] Yehuda Afek, Geoffrey Brown, and Michael Merritt. A lazy cache algorithm. In *ACM Symposium on Parallel Algorithms and Architectures*, pages 209–222, June 1989.

[76] Geoffrey Brown and Miriam Leeser. Synthesizing correct sequential circuits. In *International Conference on Computer Hardware Description Languages*, pages 169–182, June 1989.

[77] Geoffrey Brown, Mohamed Gouda, and Chuan lin Wu. A self-stabilizing token system. In *Hawaii International Conference on System Sciences*, pages 218–222, 1987.

[78] Geoffrey Brown and Chuan lin Wu. Operating system kernel for a reconfigurable multiprocessor system. In *International Conference on Parallel Processing*, pages 234–241, August 1986.

[79] Manjai Lee, Eric Fiene, Chuan lin Wu, Geoffrey Brown, and Nader Bagherzadeh. Network facility for a reconfigurable computer architecture. In *International Conference on Distributed Computing Systems*, pages 264–271, 1985.

[80] Chuan-Lin Wu, Manjai Lee, Chai Sudtikipisan, Jamshad Moaddeb, Geoffrey Brown, Woei Lin, Nader Bagherzadeh, and David Vaughn. Prototype of star architecture – a status report. In *National Computer Conference*, pages 191–201, 1985.

Reports

[81] Geoffrey Brown. Ensuring long-term access to government documents. In *International Association for Social Science Services and Technology (IASSIST)*, 2007.

[82] Geoffrey Brown. Virtualizing the CIC floppy disk project: An experiment in preservation using emulation. In *Federal Depository Library Conference*, Fall 2006.

[83] Geoffrey Brown and Lee Pike. "easy" parameterized verification of cross clock-domain protocols. In *Designing Correct Circuits*, April 2006.

[84] Geoffrey Brown. Internet address clustering for intelligent route control. 2003.

[85] Nikolay Mateev, Paolo Faraboschi, and Geoffrey Brown. An analysis of data access patterns in integer benchmarks. Technical report, HP Labs Internal Report, November 1997.

[86] Sam Weber, Bard Bloom, and Geoffrey Brown. Compiling joy into silicon: A formally verified compiler for delay-insensitive circuits. Technical Report TR96-1566, Cornell University Department of Computer Science, 1996.

[87] Alan Wenban, John O'Leary, and Geoffrey Brown. Using the promela toolset with the riopci user configurable i/o board. User Manual, August 1996.

[88] Alan Wenban and Geoffrey Brown. Multi-rate clocking for reconfigurable logic arrays. In *4th Canadian Workshop on Field Programmable Devices*, August 1996.

[89] John O'Leary, Alan Wenban, and Geoffrey Brown. A toolset for supporting systems with reconfigurable hardware. Technical Report, October 1994.

[90] Geoffrey Brown and Mirian Leeser. From programs to transistors: verifying hardware synthesis tools. In Miriam Leeser and Geoffrey Brown, editors, *Proceedings of the Mathematical Sciences Institute workshop on Hardware specification, verification and synthesis: mathematical aspects*, number 408 in Lecture Notes in Computer Science, pages 129–151, New York, NY, USA, 1990. Springer-Verlag New York, Inc.

MS/PHD Students Supervised (chair)

Zahra Tarkhani	MS, December 2017.
Kam Woods	PhD, December 2010 "Preserving Long-term Access to Government Documents in Legacy Digital Formats"
Bhanu Pisupati	PhD, August 2007 "A Virtual Filesystem Framework to Support Embedded Software Development"
Alan Wenban	PhD, August 1997 "A Software Development Environment for Real-Time systems Based on User-reconfigurable Hardware."
John O'Leary	PhD, August 1995, "A Model and Proof Technique for Verifying Hardware Compilers for Communicating Processes."
Larry Prince	MS, Fall 1994, "A Prototype Token Ring Local Area Control Network for Sensors."
Richard Chapman	PhD (CS), August 1993, "Verified High Level Synthesis."
Chee-keng Chang	MS, Summer 1990, topic "A Compiler for a High-level Hardware Description Language."
Peter DelVecchio	MS, Summer 1989, "The Design and Formal Verification of an Integrated Circuit for Use in a Floating-Point Systolic Array Fast Fourier Transform Processor."

PHD Students Supervised (minor member)

Omer Arap (CS PhD 2016), "Offloading Collective Operations to Network Aware Programmable Logic", Filipa Duarte (ECE PhD 2008 – Technical University of Delft, "A Cache-Based Hardware Accelerator for Memory Data Movements", Lee Pike (CS PhD 2006) "Formal Verification of Time-Triggered Systems", Dana Madsen (EE PhD 1997) "Dynamic cache partitioning for vector and matrix computations", Mark Charney (EE PhD 1995) "Correlation-based hardware prefetching", Bradford Glade (CS PhD 1995) "A scalable architecture for reliable publish/subscribe communication in distributed system", Mark Aagaard (EE PhD 1994) "A framework for the specification, design, and verification of pipelines with structural hazards", Russell Brown (CS PhD 1994) "Localization, mapmaking, and distributed manipulation with flexible, robust mobile robots", Mark Linderman (EE PhD 1994) "Simulation of digital circuits in the presence of uncertainty", William Rucklidge (CS PhD 1994) "Efficient visual recognition using the Hausdorff distance", Mayan Moudgill (CS PhD 1993) "Implementing and exploiting static speculation on multiple instruction issue processors", Christos Zoulas (PhD 1991) "A general purpose rasterization processor"

MEng and Undergraduate Project Students

MEng Students – Natasha Avila, William Bogdel, Richard Hammerstone, Glen Bartolini, Matt Fisch, Dawn Hergenhan, Anitruth Hiranraks, Bennett Ih, Perry Kamel, Jaidi Khalil, Minjung Kim, Paul Look, Kolawole Otitoju, Anthony Poon, Doug Rosich, Douglas Smith, Siu Kwan Tsang, Steve Thenell, Fadi Zuhayri

Undergraduate Senior Projects – Ivan Bachelder, Mike Bracken, Scott Casavant, Sujai Chari, Gerald Cheung, Frances Donate, Leslie Farkus, Thomas Jackson, Sin-Kuen Ko, Jesse Lackey, Paul Look, Doug Nortz, Parissa Mohamadi, Ralph Mor, Ted Nelson, Tony Su

Selected Invited Lectures

IMAL, Brussels, *Sustainable Emulation for Long-Term Preservation of Digital Artifacts*, October 2015.

Workshop on Software Infrastructure for Reproducibility in Science, NYU, *Accessing Born-Digital Materials in the Face of Technical Obsolescence*, May 2013.

Indiana University Institute for Digital Arts and Humanities *Accessing Born-Digital Materials in the Face of Technical Obsolescence*, April 2012.

University of North Carolina School of Information and Library Science, *Enabling Long-term Access to Born-Digital Materials on CD-ROMS: Migration , Emulation, and an Imperative to Pool Technical Knowledge*, March 2011.

University of Illinois Graduate School of Library and Information Science, *Enabling Long-term Access to Born-Digital Materials on CD-ROMS: Migration, Emulation, and an Imperative to Pool Technical Knowledge*, February 2011.

National Library of the Netherlands (Koninklijke Biblioteek), *Virtualizing the CIC Floppy Disk Project: An Experiment in Preservation Using Emulation*, November 2006.

Indiana University Logic Seminar *"Easy" Parameterized Verification of Cross Clock Domain Protocols,* October 2005.

Technical University of Delft, *On-chip File Systems to Support SoC Software Development,* January 2005.

University of Utah Computer Science Department, *Internet Address Clustering for Intelligent Route Control*, February 2003.

University of California Davis Electrical Engineering Department, *Internet Address Clustering for Intelligent Route Control*, February 2003.

McGill University Computer Science Department, *Internet Address Clustering for Intelligent Route Control*, February 2003.

Washington University Computer Science Department, *Internet Address Clustering for Intelligent Route Control*, February 2003.

Indiana University Computer Science Department, *Internet Address Clustering for Intelligent Route Control*, Fall 2002.

HP Embedded Workshop, *Scalability and Customization in the Lx Embedded Processor Family* with P. Faraboschi, 1999.

HP Integrated Circuits Business Unit, *Accurate LISARD Icache Simulation*, April 1997.

HP Laboratories, *Exploring "Custom" in CVLIW*, February 1997.

Northeastern University, *User Configurable Data Acquisition Systems,* November 1996.

Hewlett Packard Labs, *User Configurable Data Acquisition Systems,* October 1996.

Xilinx Workshop on Reconfigurable Computing, *Data Acquisition Systems with User Configurable Hardware,* July 1996.

Rome Laboratories, *Hardware Compiler Verification – An Exercise in Combining Model Checking and Algebraic Laws in Large Scale System Verification,* spring 1996.

Cornell University EE Colloquium, *Data Acquisition Systems with User Configurable Hardware*, September 1995.

Oxford University, "Compiling Concurrent Programs Into Delay Insensitive Circuits," Fall 1993.

Southbank University, "Compiling Concurrent Programs Into Delay Insensitive Circuits," Fall 1993.

Gronigen University, "Compiling Concurrent Programs Into Delay Insensitive Circuits," May 1993.

GMD – Bonn, Germany, "Compiling Concurrent Programs Into Delay Insensitive Circuits," May 1993.

Xerox PARC, *Compiling Programs into Delay-Insensitive Circuits,* May 1992.

University of Texas, *Towards Truly Delay-Insensitive Circuit Realizations of Process Algebras,* November 1991.

University of Waterloo, *Towards Truly Delay-Insensitive Circuit Realizations of Process Algebras,* June 1991.

AT&T Bell Laboratories, *Self-Stabilization Over Unreliable Communication Media,* May 1991.

Washington University in St. Louis, *Towards Truly Delay-Insensitive Circuit Realizations of Process Algebras,* December 1990

Bucknell University, *An Introduction to Communication Protocols,* October 1990.

Programming Research Group, Oxford University, *Self-stabilization over Unreliable Communication Media,* September 1990

NASA Goddard Space Flight Center, *From programs to transistors: verifying hardware synthesis tools,* August 1989

Department of Computer Sciences, University of Texas at Austin, *Lazy Caches,* April 1989

IBM T.J. Watson Research Lab, *Self-stabilizing token systems,* November 1988

Programming Research Group, Oxford University, *Self-stabilizing token systems,* July 1988

AT&T Bell Laboratories, *Self-stabilizing token systems,* June 1988